Gooch & Housego

MODEL NUMBER:

(R) 64020-200-2ADMDFS-A

SPECIFICATIONS

Document Number: **56A18641E**

A Digital Frequency Synthesizer OEM Module with Analog and Digital Modulation input and a 2 Watt RF Output. When specified as R64020-200-2ADMDFS-A, the unit delivered will be manufactured to be compliant with EU Directive 2002/95/EC for **R**eduction **o**f **H**azardous **S**ubstance.

PARAMETER	**SPECIFICATION**
Bandwidth:	20 – 200 MHz typical
Clock Frequency:	1000 MHz
Step Size:	< 1 Hz with 30 Bits input
Frequency Settling Time:	250 ns Maximum
Power Out:	2 watts typical
Harmonic Distortion: 2^{nd}:	-20 dBc Maximum
3^{rd}:	-15 dBc Maximum
Analog Modulation:	0 to +1 volt Analog into 50 Ω, +1volt = Full RF power output.
Digital Modulation:	TTL levels TTL Active High = Full RF output power TTL Active Low = Minimum RF output power No Signal = Full RF output power (pulled high internally)
Rise and Fall Time:	20 ns
Extinction Ratio:	
Digital:	30 dB Minimum
Analog:	40 dB Minimum
Reference Out:	A reference signal from the un-modulated output of the synthesizer. +0 dBm nominal
Applied Power:	+ 28 volts DC @ 1 amp Maximum + 3.3 volts DC @ 1 amp Maximum
MAXIMUM RATINGS:	
Ambient Temperature:	40^0 C
RF Output:	No DC Feedback
Supply Voltage:	30 volts DC 3.5 volts DC
INPUT / OUTPUT CONNECTIONS:	
+28v, +3.3V, and Gnd	Filtered Feedthru
Mod In	SMC Male
Reference Out	SMC Male
RF Output	SMA Female
"FREQUENCY SELECT" Control	TTL 30 bit binary word, Digital Modulation Input, Reset, and a Latch control input through the 37 pin D sub connector. See page 2 for pinout.
Outline Drawing	53D3887

64020-200-2ADMDFS-A

"FREQUENCY SELECT" PIN OUT

37-PIN MALE D-SUB CONNECTOR

PIN			PIN	
1	FS_0	LSB	20	FS_1
2	FS_2		21	FS_3
3	FS_4		22	FS_5
4	FS_6		23	FS_7
5	FS_8		24	FS_9
6	FS_{10}		25	FS_{11}
7	FS_{12}		26	FS_{13}
8	FS_{14}		27	FS_{15}
9	FS_{16}		28	FS_{17}
10	FS_{18}		29	FS_{19}
11	FS_{20}		30	FS_{21}
12	FS_{22}		31	FS_{23}
13	FS_{24}		32	FS_{25}
14	FS_{26}		33	FS_{27}
15	FS_{28}		34	FS_{29} MSB
16	Latch		35	Digital Modulation Input (Active High)
17	Master Reset (Active High)		36	N/C
18	N/C		37	N/C
19	Ground			

$$\text{Control Word } K_{10} = \frac{F_{OUT\,(Hz)}(2^{31})}{F_{OSC\,(Hz)}} \text{ in Decimal notation}$$

CONTROL WORD CALCULATIONS

The output frequency and step size is a function of the clock rate and the "FREQUENCY SELECT" data. The output frequency can be calculated from the formula:

$$f_{out} = \frac{(f_c)\,(k_{10})}{2^n}$$

Where: f_c = clock frequency in Hz
k_{10} = input word in decimal notation
n = 31 *See note below.

The minimum output frequency and step size are given by:

$$f_{min} = \frac{f_c}{2^n}$$

An example of setting the frequency:
Clock frequency = 1000×10^6 Hz
Desired output frequency = 30.00×10^6 Hz

$$K_{10} = \frac{f_{OUT\,(Hz)}(2^{31})}{f_{OSC\,(Hz)}}$$

$$K_{10} = \frac{30 \times 10^6\,(2^{31})}{(1000 \times 10^6)}$$

$K_{10} = 64424509.44$ Decimal

Convert K_{10} to HEX \/- MSB \/ - LSB

K_{HEX} = 3D70A3D → 03D70A3D -Setting for front panel "HEX" switches
NOTE: The switches on the front panel of the driver are LSB to MSB - right to left.

Convert K_{HEX} to Binary \/ LSB - pin1

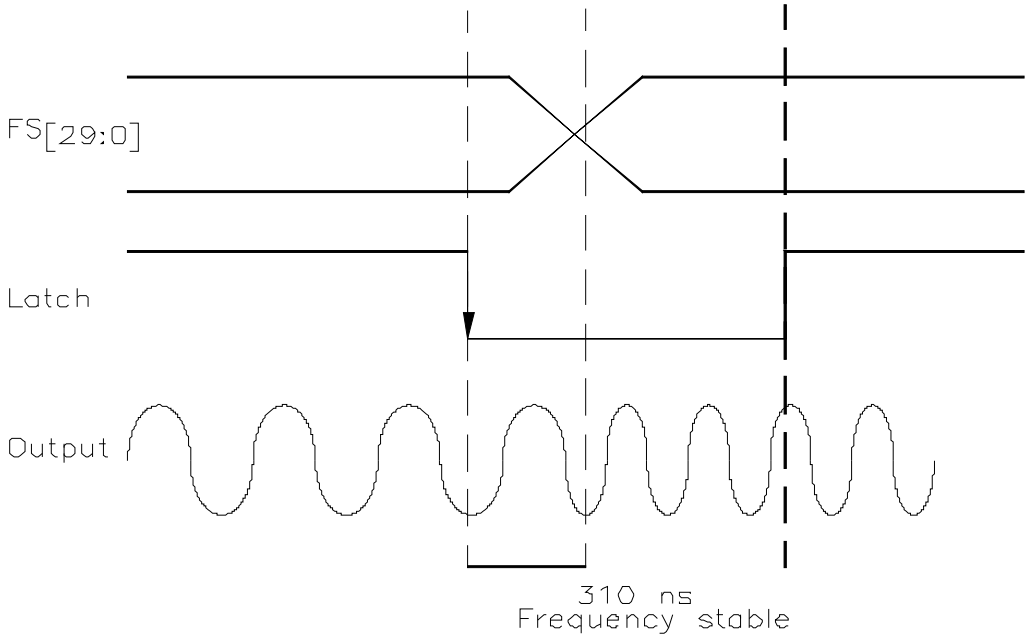
K_B = 0000111101011100001010001111 01 -Setting for binary word input to back panel "FREQUENCY SELECT" 37 pin D-sub connector
/\
These 4 bits are added to complete the 30 bit word

*Note: This system only uses 30 bits to set the frequency output from the driver. The accumulator inside the chip is 31 bit, so use 2^{31} in your calculations for precision.

The LATCH function (pin 16) is a TTL compatible input which is used to load new frequency information into the driver. Frequency data is loaded into the driver when the signal on the LATCH pin goes from HIGH to LOW (falling edge).

Master RESET is a TTL active HIGH and resets the accumulator to zero, ie, no frequency output, when a TTL HIGH is applied to pin 17. This is pulled LOW via. a 1 KΩ resistor.

To generate a single frequency, apply the binary frequency word to the FS input, A falling edge on the LATCH input will then load the data and change the frequency.



To generate a ferquency chirp, set the starting frequency as above and then apply the delta word to the FS input. A falling edge on DLATCH will then load the delta frequency word and initiate the chrip. The chirp will stop and output will return to to starting value or a rising edge.