introspect technology

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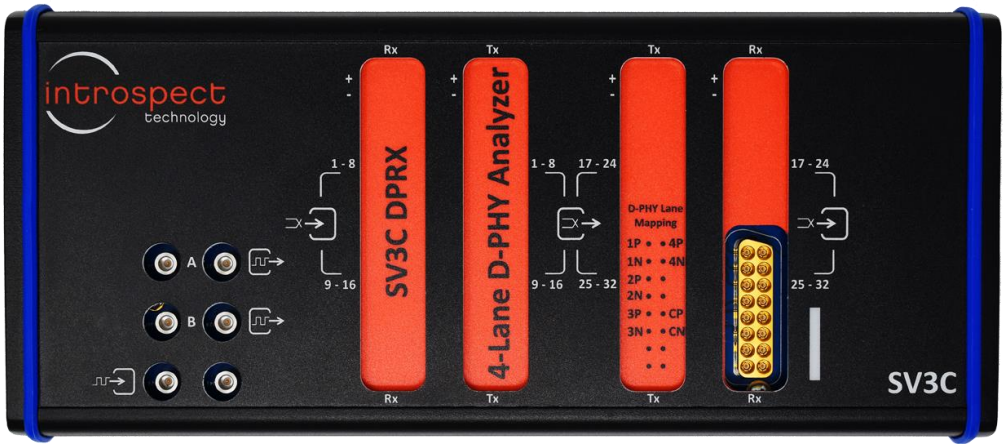
DATA SHEET

SV3C-DPRX

MIPI D-PHY Analyzer

C SERIES



Published in Canada on December 13, 2021
EN-D004E-E-21347

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Introduction

OVERVIEW

The SV3C-DPRX D-PHY Analyzer is an ultra-portable, high-performance instrument for exercising and validating MIPI D-PHY transmitters as well as probing live MIPI D-PHY links. The Analyzer is data-rate agile, making it ideal for the capture and analysis of MIPI transmitters used in cameras, displays, and other devices. It also includes integrated LP and HS receivers, dynamic termination, and offers sophisticated capture, compare, and analysis modes.

The D-PHY Analyzer operates using the highly versatile Introspect ESP Software environment that allows for automating transmitter tests such as CRC error counting or PHY/protocol timings.

This document includes electrical specifications of the Analyzer and provides details on the various methods for the capture and analysis of D-PHY traffic. Please refer to the Help Menu within the Introspect ESP Software for additional operating instructions.

KEY FEATURES

- Physical layer validation of MIPI D-PHY transmitters
- Protocol analysis for CSI-2, DSI, and DSI-2
- IP and software validation testing
- Debug of active D-PHY links
- Interface test
- Plug-and-play system-level validation

KEY BENEFITS

- Any-rate operation
- Flexible lane assignment
- Protocol Analyzer suite for CSI-2, DSI, and DSI-2
- Video frame extraction
- Precision time stamps to help understand each physical layer event
- Advanced triggering based on physical-layer or protocol-layer events
- Continuous monitoring mode for long-term error checking

- Programmable trigger I/O
- Analog signal measurement across 4 lanes
- Intuitive state-of-the-art Python programming environment

ORDERING INFORMATION

TABLE 1: ITEM NUMBERS FOR THE SV3C-DPRX AND RELATED PRODUCTS

PART NUMBER	NAME	KEY DIFFERENTIATORS
4585	SV3C-DPRX - SV3C D-PHY Analyzer Bundle (this product)	Covers the MIPI D-PHY physical layer
4590	SV3C-DPRXCPRX - SV3C Combo C-PHY/D-PHY Analyzer Bundle	Combo D-PHY and C-PHY capability
4594	SV3C-DPRX Upgrade	Firmware and software license upgrade from 4585 to 4590

Feature Description

COMPLETE D-PHY RECEIVER IMPLEMENTATION

The SV3C-DPRX is a complete, integrated, 4-lane D-PHY receiver providing the analog front-end circuitry for D-PHY as well as a complete protocol back-end. As shown in Figure 1, each lane contains low power (LP) threshold voltage detectors, dynamically controlled D-PHY termination resistors, and fully differential high speed (HS) receivers. The real-time behavior of the DPRX enables broad acquisition capabilities on physical-layer and protocol-layer events as detailed in Figure 2. The figure illustrates two common setups for deploying the DPRX, which can be used as either a terminating receiver or to probe live links.

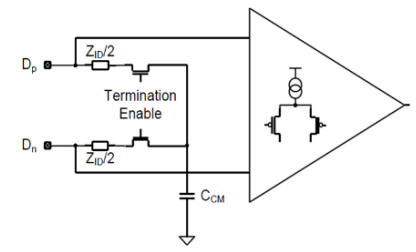


Figure 1: SV3C receiver illustration showing automatic termination switches.

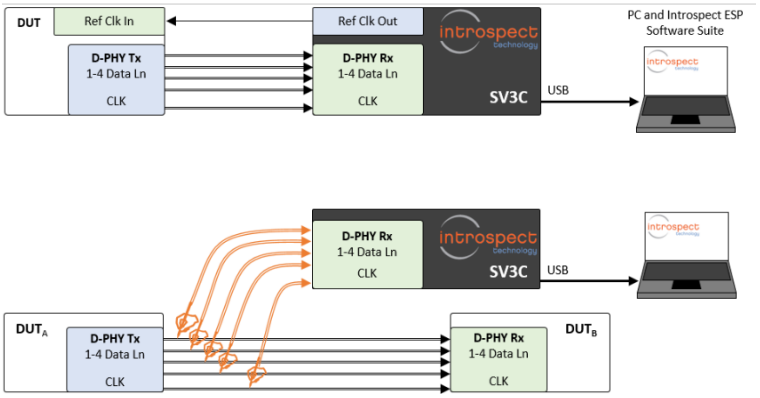


Figure 2: (a) Illustration of the DPRX as a terminating end-point receiver, or (b) while probing a complete D-PHY link.

PROTOCOL ANALYSIS AND PRECISION TIME STAMPS

The SV3C-DPRX is a complete protocol analyzer for both camera and display serial interfaces. Either protocol can be selected within a single session, and the analyzer automatically adjusts its viewer displays based on the protocol being measured (Figure 3). At the same time, irrespective of the protocol, five viewers provide insight into PHY and protocol events while hyperlinks make for quick and intuitive navigation across the layers, namely:

HS Bursts – View each high-speed burst, by lane, with quick statistics of the time of arrival in nanoseconds, SOT offset and captured bits in each

CSI/DSI Packets – Merged traffic from all lanes is shown as unique packets. Headers are decoded for easy, high-level viewing, and errors (CRC, ECC1, ECC2) are automatically highlighted

LP States – Each LP state is captured along with its time of arrival and duration; this viewer is extremely effective for building a visualization of the physical layer events

Frame Viewer – Images are automatically reconstructed, even if incomplete, with details such as pixel format, virtual channel, and image dimensions

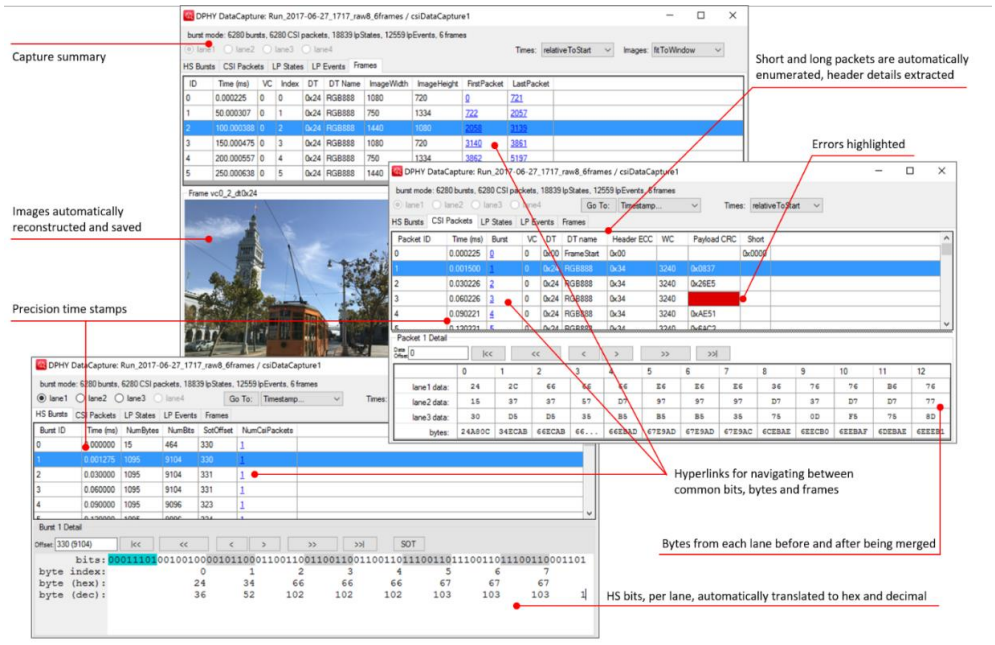


Figure 3: Protocol analyzer views.

To enable the acquisition of high-definition video streams under realistic traffic conditions, the SV3C-DPRX relies on event-based captures, assigning a time stamp to each pertinent event of the physical layer and protocol layer. This allows for optimized data storage and extremely efficient long-term data analysis. In terms of display, each viewer contains a column dedicated to the precision time stamps of a given burst, packet, LP event or frame. Correlating events in time makes it easy to identify anomalous transitions, unexpected short- or long-packets, and other physical layer perturbations, as depicted in Figure 3.

HARDWARE CRC CHECKING AND PACKET ERROR RATE TESTING

Another fundamental feature of the SV3C-DPRX D-PHY Analyzer is hardware-based packet error-rate detector. Similar to traditional BER, the PERT enables the measurement of real D-PHY transmissions from CSI generators or DSI generators. As illustrated in Figure 4, the Analyzer detects and filters all signal waveforms and compares only the packet data transmitted between SOT and EOT, registering errors after the data has been merged between lanes, thereby comparing errors in packets rather than bits.

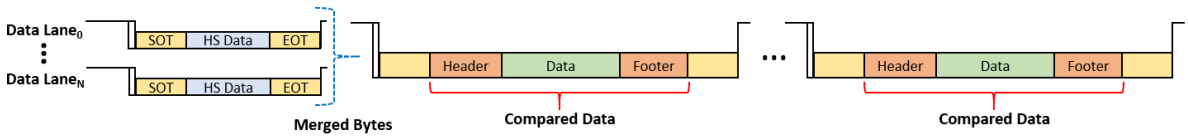


Figure 4: Illustration of packet error rate testing.

ADVANCED TRIGGER MODES

Figure 5 shows the user interface for defining the trigger mechanisms within the Analyzer. At the highest level, the Analyzer can be programmed to perform immediate captures (in which all data is measured irrespective of whether there are LP transitions or not) or burst-mode captures (Figure 6). The benefit of the immediate capture mode is that it allows for pattern learning and detecting multiple non-deterministic / non-repetitive packets. On the other hand, triggered captures offer a more focused view of D-PHY global timing parameters. In this mode, the D-PHY Analyzer sets the termination resistors into automatic mode. Then, the analyzer waits for a valid LP to HS entry sequence before enabling a capture. If no valid HS-entry transition is detected, the capture returns an empty array. However, when a valid HS-entry transition is detected, the capture starts immediately.

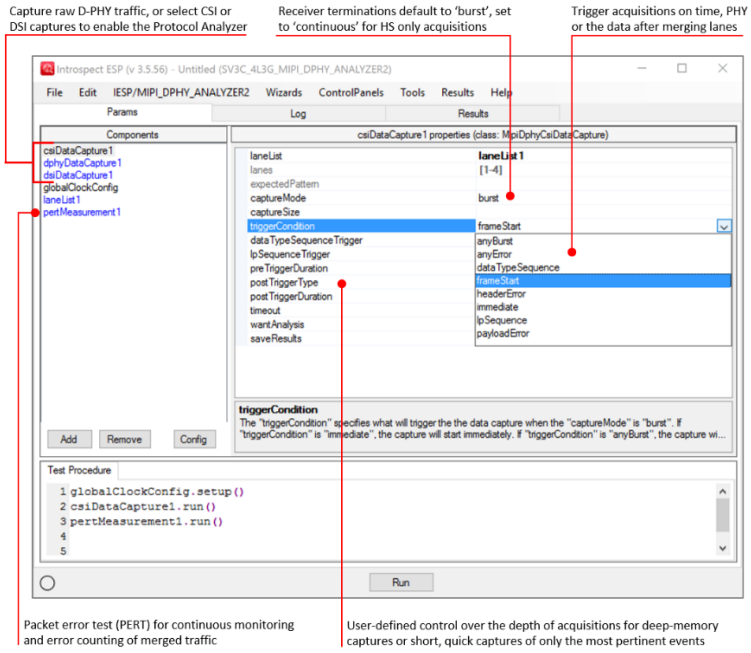


Figure 5: Introspect ESP GUI for the SV3C-DPRX. Top left: Components, shows CSI, DSI and PHY data acquisition methods. Top right: Properties, showing CSI Data capture. Bottom: test procedure ready to execute a CSI Data Capture, then PERT.

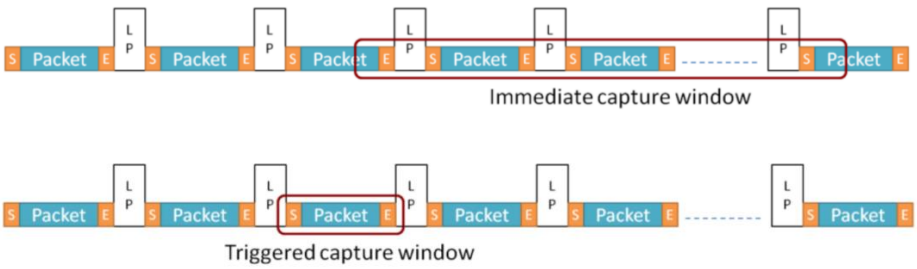


Figure 6: Illustration of multi-packet, per-lane PHY-level capture (Top), and triggered packet capture (Bottom).

Acquisitions and their depth are defined in time, by PHY events or by bytes of merged high-speed traffic. Figure 7 illustrates two methods of triggering acquisitions by PHY events. In Figure 7 (top), an acquisition begins on the first high-speed burst witnessed and completed after user-defined N bursts are recorded. In Figure 7 (bottom), a capture begins immediately and the Analyzer records for a user-defined period of N nanoseconds. Figure 8 illustrates three examples of triggering acquisitions on merged, high-speed data. The DPRX supports one to four data lanes and independently merges and monitors bytes. Acquisition start is user-defined as the first event observed: (a) error within a packet header, (b) variable data type identifier, here chosen as 0x01 and (c) frame start packet (CSI only). The depth of the acquisition for each is arbitrarily chosen according to the number of N received: (d) bursts, (e) bytes and (f) frame end packets.

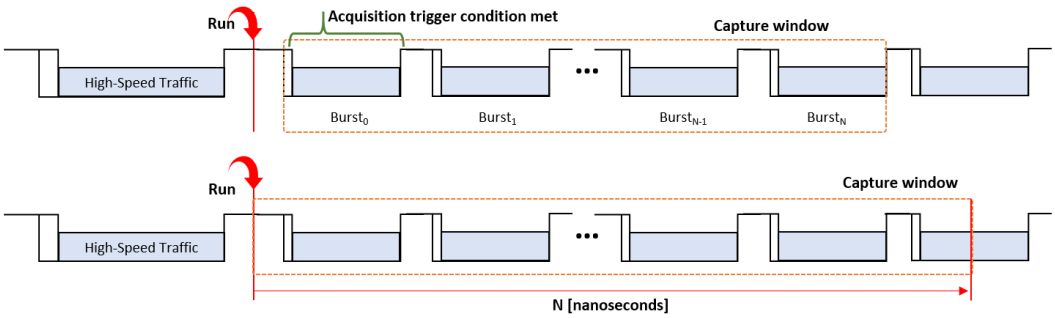


Figure 7: Illustration of two PHY-based acquisitions. Above, recording is triggered on first observed burst and depth is determined by user-defined N bursts. Below, acquisition begins immediately, and depth is for a user-defined period of N nanoseconds.

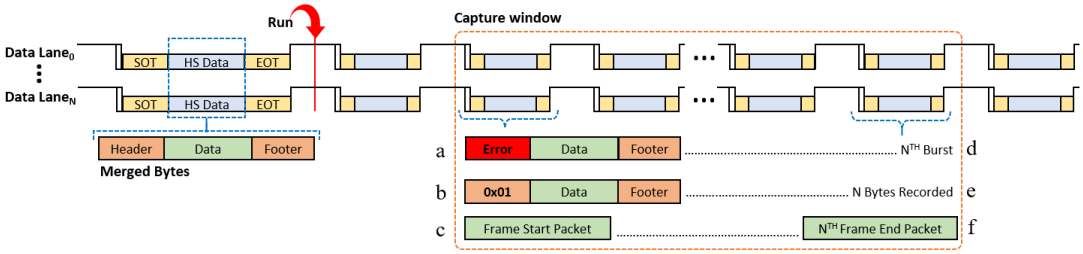


Figure 8: Illustration of three acquisitions triggered on merged high-speed traffic events: (a) header error, (b) user-defined data type identifier and (c) frame start packet. Three methods of acquisition depth are shown: (d) user-defined N bursts, (e) bytes, and (f) frames.

Finally, for completeness, Table 2 and Table 3 provide a list of trigger mechanism that are available in the Analyzer.

TABLE 2: DPRX METHODS FOR TRIGGERING A D-PHY ACQUISITION.

TRIGGERCONDITION	TYPE	TRIGGER DESCRIPTION
anyBurst	PHY	the first high-speed burst witnessed over any data or clock lane
immediate	Time-base	time-base acquisition, beginning immediately when run
lpSequence	PHY	user-defined sequence of LP states, e.g. "11,01,00" reflects a proper LP-HS entry sequence
anyError	CSI, DSI	the first error is registered: header, CRC or payload
dataTypeSequence	CSI, DSI	user-defined integer value to be identified in a packet header
headerError	CSI, DSI	protocol layer, the first error recognized in a packet header
payloadError	CSI, DSI	protocol layer, the first error recognized in a packet payload
frameStart	CSI	CSI-only, any packet with header data type 0x00 indicating the beginning of a frame
verticalSyncStart	DSI	DSI-only, any packet with header data type 0x01 indicating the beginning of a frame

TABLE 3: UNITS AVAILABLE FOR DEFINING DEPTH OF AN ACQUISITION, ACCOMPANIED WITH A USER-DEFINED VALUE.

POSTTRIGGERTYPE	TYPE	DESCRIPTION
durationInNs	Time-base	time-base acquisition, defined in nanoseconds
numberOfBursts	PHY	the total number of unique bursts acquired, across all data lanes
numberOfBytes	PHY	the total number of bytes recorded between SOT and EOT of all bursts
numberOfLpCommands	PHY	the first error is registered: header, CRC or payload
numberOfLpStates	PHY	number of unique LP states, e.g. "11,01,00" would be 3
nuberOfFrameEnds	CSI	protocol layer, the number of frame-end packets recorded
numberOfVerticalSyncStarts	DSI	protocol layer, the number of packets with data type identifier 0x01

ANALOG PARAMETER MEASUREMENT

The SV3C-DPRX D-PHY Analyzer includes inventive sampling technology that allows for analog parameter measurement of both the LP portion of a D-PHY signal waveform and the HS portion. Simply enable Burst-Mode Analog Capture, and the SV3C D-PHY Analyzer will automatically measure LP-to-HS transitions and HS-to-LP transitions just like an oscilloscope. Moreover, the SV3C D-PHY Analyzer can measure waveforms both in a differential manner (P voltage minus N voltage) and in a single-ended manner. Figure 9 shows examples of both measurement modes. On the left of Figure 9, the difference between P and N is displayed, and this is why the LP state transitions appear this way: LP-11 is zero when measured differentially, LP01 is a large negative value when measured differentially, and LP-00 is zero again. To the right of Figure 9, the single-ended waveform of P is displayed. Note that these measurements are not acquired simultaneously.

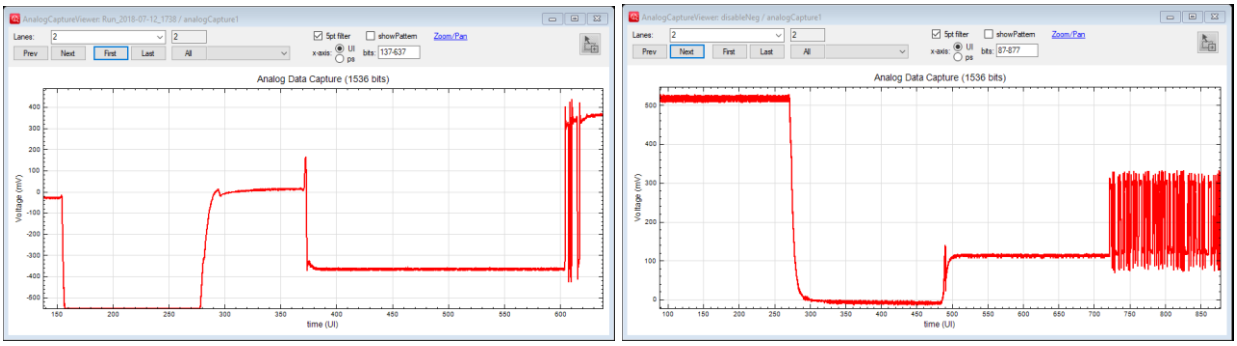


Figure 9: Illustration of analog waveform capture on live CSI-2 frame transmissions. On the left, the differential waveform (P-N) is displayed, and on the right, the single ended waveform (P) is displayed.

AUTOMATION

The SV3C-DPRX D-PHY Analyzer is operated using the award-winning Introspect ESP Software, a Python-based scripting environment. Shown in Figure 10, it includes a comprehensive suite of components and methods for executing capture and analysis of D-PHY transmissions, and a canvas for automating test procedures and rich analysis. The Python library is open, and an optional .NET DLL library provides access for integration with DUTs, other test equipment using Python, or alternative programming languages.

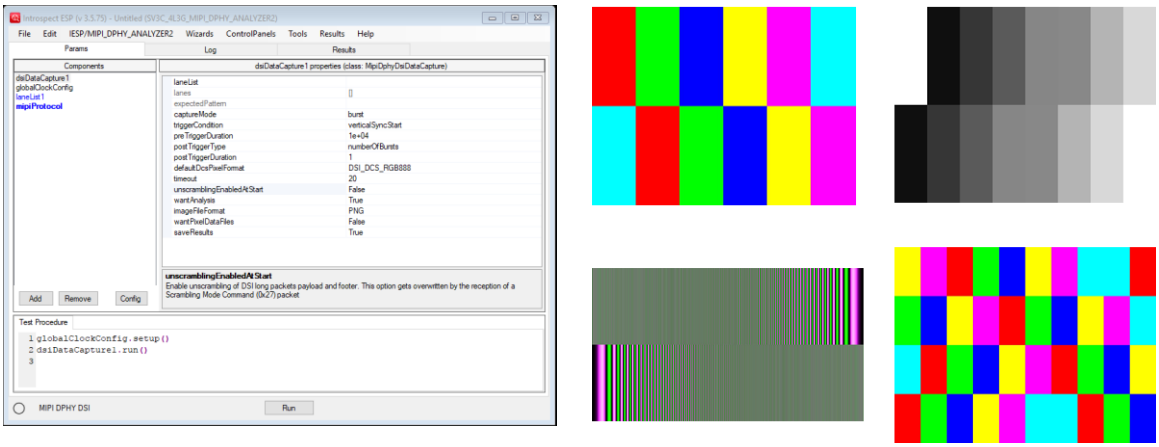


Figure 10: Introspect ESP Software environment, left, and right, examples of image captures.

Physical Description and Pinout

Figure 11 shows the physical connections of the SV3C MIPI D-PHY Analyzer. A single HUBER+SUHNER MXP connection provides input for the high-speed D-PHY lanes: four data lanes and one clock (MXP to SMA-Female breakout cable included). Differential SMP connections for reference clock output and input are available for synchronization with devices under test (DUT). A 240-pin SEARAY connection, depicted in Figure 12, provides programmable GPIO for various purposes such as:

- Low-speed communications with DUT via SPI or I2C
- Programmable trigger outputs based on real-time events such as errors, bursts or received data patterns
- Trigger input for data acquisition

Finally, Table 4 shows the pin mapping on the MXP connector.

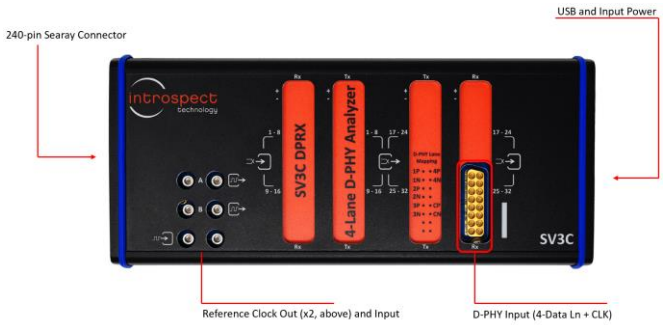


Figure 11: SV3C MIPI D-PHY Analyzer connections.

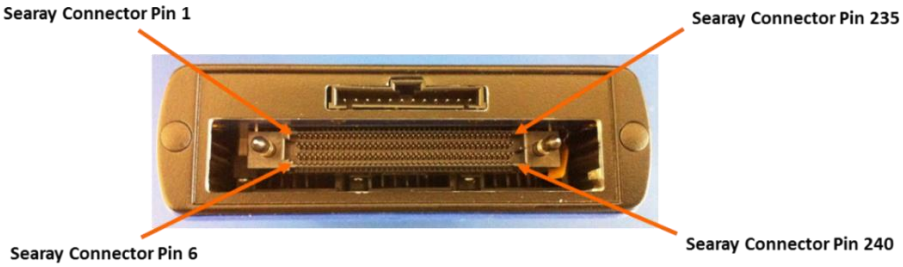
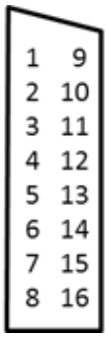


Figure 12: Illustration of the 240-pin SEARAY connector.

TABLE 4: MAPPING OF LOWER MXP CONNECTOR (LANE PINOUT).

	CONNECTOR PIN NUMBER	CORRESPONDING RX LANE
	1,2	Lane 1 (P,N)
	3,4	Lane 2 (P,N)
	5,6	Lane 3 (P,N)
	9,10	Lane 4 (P,N)
	13, 14	CLK (P,N)

Specifications

TABLE 5: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol			
Physical Layer Interface	D-PHY		Version 1.2, 2.0
MIPI Protocol	CSI, DSI		CSI-2 v1.3, v2.0, v3.0, DSI-2 v1.1
LS/HS Handling	Automatic		
Compression	VESA		Version 1.2
ALP Mode	Yes		
Ports			
Number of D-PHY Lanes	4		With one high speed clock lane
Number of Dedicated Low-Speed Output Reference Clocks	2		Individually synthesized frequency and output format
Number of Dedicated Input Reference Clocks	1		Used as external reference clock input
Number of GPIO pins	6		Via Molex connector
Number of I2C/I3C Masters	1		Via Molex connector
Connections to PC for Introspect ESP Software Control	2		USB2 (module control) USB3 (data transfer)
Power Consumption			
DC Input Voltage	12	V	
Power Dissipation	< 60	W	

TABLE 6: D-PHY DATA RATES AND REFERENCE CLOCKS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Data Rates / Frame Rates			
Minimum HS Data Rate	50	Mbps	Per Lane
Maximum HS Data Rate	3.125	Gbps	Per Lane
Frequency Resolution of HS Data Rate	1	kbps	
Minimum LP Toggle Rate	0	MHz	
Maximum LP Toggle Rate	20	MHz	
Reference Clock Frequencies			
Minimum External Input Clock Frequency	10	MHz	
Maximum External Input Clock Frequency	250	MHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)
Minimum Output Clock Frequency	10	MHz	
Maximum Output Clock Frequency	250	MHz	
Output Clock Frequency Resolution	1	kHz	
Supported External Output Clock I/O Standards			LVDS, LVPECL, CML, HCSL, and LVCMOS

TABLE 7: D-PHY RECEIVER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Input Coupling			
Input Impedance	50	ohm	HS transmission, each wire
Input Impedance	Hi-Z		LP transmission
HS / LP Voltage			
Minimum $\|V_{ID}\|$	90	mV	At SV3C MXP connector
Maximum $\|V_{ID}\|$	600	mV	At SV3C MXP connector
HS Threshold Voltage Measurement Accuracy	Larger of: 15% or 25 mV		-225 mV to +225 mV input range
Minimum Programmable LP Threshold Voltage	0	mV	
Maximum Programmable LP Threshold Voltage	1300	mV	
Programmable LP Threshold Voltage Resolution	1	mV	
LP Threshold Measurement Accuracy	25	mV	50 mV to 1300 mV input range
Resolution Enhancement and Equalization			
Minimum DC Gain	0	dB	
Maximum DC Gain	8	dB	
DC Gain Control			Per receiver
Equalization Control			Per receiver

TABLE 8: D-PHY RECEIVER TIMING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Internal Time Base			
Number of Internal Frequency References	1		
Internal Time-base Frequency Generation Accuracy	1.0	ppm	
Frequency Resolution of Received Data Rate	1	kbps	
Received Data Rate Timing Measurement Accuracy	40	ppm	
Timing Generator Performance			
Timing Resolution	7.8125	mUI	
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	Unlimited		
Global Timing Performance			
Minimum T_{LPX}	50 ns		
Minimum $T_{HS-PREPARE}$	40 ns + 4 UI		
Minimum $T_{HS-PREPARE}$ + $T_{HS-ZERO}$	145 ns + 10 UI		
Minimum $T_{HS-TRAIL}$	Larger of: (60 ns + 4 UI) or 8 UI		
Minimum $T_{CLK-PREPARE}$	38 ns		
Minimum $T_{CLK-PREPARE}$ + $T_{HS-ZERO}$	300 ns		
Minimum $T_{CLK-PRE}$	8 UI		
Minimum $T_{CLK-POST}$	60 ns + 52 UI		
Minimum $T_{CLK-TRAIL}$	60 ns		

TABLE 9: PATTERN HANDLING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Features			
Supported Pixel Formats (CSI)	RAW, RGB, YUV		RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20, RGB444, RGB555, RGB565, RGB666, RGB888, YUV420, YUV422
Supported Pixel Formats (DSI)	RGB YCbCr		RGB101010, RGB121212, RGB332, RGB565, RGB666, RGB888, YCbCr420_12bit, YCbCr422_16bit, YCbCr422_20bit, YCbCr422_24bit
Decompression Support (DSI)	Yes		DSC, V-DCM
Display Command Set (DSI) Support	Yes		
Memory Depth	4	GByte	For received packet data

TABLE 10: PACKET AND FRAME ANALYSIS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Features			
HS Data Rate Detection	Yes		Automatic
CSI / DSI Packet Analysis	Yes		Header, Payload, ECC extraction, data type detection, virtual channel support
Frame Analysis	Yes		Image width / height detection Pixel format and frame rate detection
CRC and ECC Analysis	Yes		Payload error and header error detection, Packet error statistics
Trigger Conditions for Data Capture	Yes		Refer to Table 2
Specification of Data Acquisition Duration	Yes		Refer to Table 3

TABLE 11: PERT ANALYSIS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
PERT Characteristics			
Maximum Packet Size	$2^{32} - 1$		
Maximum Number of Packets	$2^{32} - 1$		
Maximum Number of Repeats	$2^{32} - 1$		
Maximum Time Between SOT in Burst Mode	1	ms	

TABLE 12: GPIO AND I2C BUS VOLTAGE CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Voltage			
Voltage Level	2.5	V	All GPIOs operate at 2.5 V LVCMOS
V_{IL} minimum	-0.3	V	
V_{IL} maximum	0.7	V	
V_{IH} minimum	1.7	V	
V_{IH} maximum	2.5	V	
V_{OL} maximum	0.4	V	
V_{OH} minimum	2.0	V	

TABLE 13: PHYSICAL CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Dimensions			
Length	9.5, 242	in, mm	
Width	4.25, 108	in, mm	
Height	1.3, 34	in, mm	
Weight	2	lbs	
Physical Connections			
Lane 1 to Lane 4, Clock	MXP		Huber & Suhner, 16 pin
GPIO and I2C			Available through 12 pin header Molex 15-91-2125
Ref Clock In	SMP		SMP Differential Pair
Ref Clock Out	SMP		SMP Differential Pair
PC connection	USB2 USB3		USB2.0 mini B USB3.0 micro B
Power Switch / Connector			AC adapter provided 110/220 V, 50/60 Hz

REVISION NUMBER	HISTORY	DATE
1.0	Import from CPRX v1.1	June 7, 2014
1.1	Updated document template	June 3, 2015
1.2	Updates to Protocol Analyzer	July 6, 2017
1.3	Updates to text	August 24, 2017
1.4	Updates to measurement features	November 23, 2018
1.5	Updates to specifications, document template updates	December 13, 2021

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Published in Canada on December 13, 2021
EN-D004E-E-21347

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