introspect technology

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DATASHEET

SV5C-eDP Analyzer

Embedded DisplayPort Analyzer

C SERIES

Published in Canada on August 22, 2024
EN-D027E-E-24235

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Introduction

OVERVIEW

The **SV5C-eDP Embedded DisplayPort Analyzer** is an ultra-portable, high-performance instrument capable of analyzing traffic for Embedded DisplayPort and DisplayPort applications. The SV5C-eDP Analyzer may be used as either a DisplayPort sink device (for source testing) or as a probing solution for capturing protocol traffic on a DisplayPort bus. The Analyzer can capture live traffic, decode symbols, detect display parameters, and extract full video frames. All these functions are integrated into Introspect's award-winning software environment, Pinetree. Figure 1 below illustrates a typical application of the SV5C-eDP Analyzer connected to an Embedded DisplayPort Source.

KEY FEATURES

- **Protocol:** supports Embedded DisplayPort (eDP) up to v2.0 and DisplayPort (DP) up to v2.1, including 8b10b encoding (HBR rates) and 128b132b encoding (UHBR rates)
- **Supported Data Rates:** up to 10.1 Gbps, including bus probing applications with Introspect's RSH2 and PV2 active probes
- **Lane Count:** configurable from 1 to 4 lanes (ML1 to ML4) plus auxiliary channel (AUX)
- **Data Capture:** extensive triggering functions and consecutive frame capture capabilities
- **Diagnostics:** full video frame extraction including standard event and symbol tables for visual analysis and data collection.

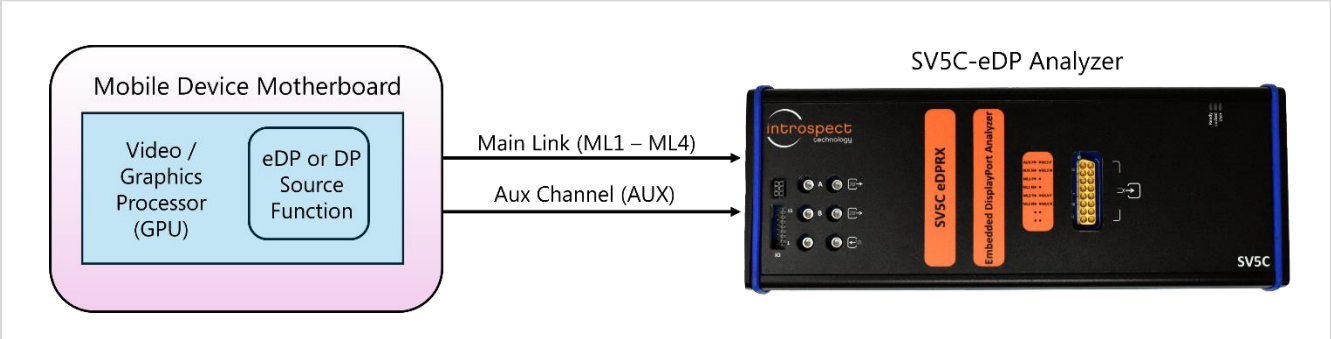


Figure 1: Typical application of the SV5C-eDP Analyzer connected to an Embedded DisplayPort system.

ORDERING INFORMATION

TABLE 1: ITEM NUMBERS FOR THE SV5C-EDP ANALYZER WITH RELATED PRODUCTS

PART NUMBER	NAME	KEY DIFFERENTIATORS
5740	SV5C-eDP Analyzer (includes Pinetree software license)	High performance eDP protocol analyzer and source tester
7154	PV2 Universal 8 GHz Universal Active Probe	8 GHz active probe that is compatible with any 50 Ohm instrument
7155	PV2PSU PV2 Power Supply Unit	Power supply for PV2
7104	RSH2 Remote Sampling Head	Integrated remote sampling head for Embedded DisplayPort bus probe applications
6312	DisplayPort Chassis Probe with Type C Interface (Includes Sensing Probe)	Connectorized DisplayPort 1:2 Fanout / Chassis Probe
6313	DisplayPort Chassis Probe with Standard DisplayPort Connector Interface (Includes Sensing Probe)	Connectorized DisplayPort 1:2 Fanout / Chassis Probe

ADDITIONAL DOCUMENTATION

PV2 Universal Active Probe Datasheet

- MK-D035E-E-23163 – PV2 8 GHz Active Probe Data Sheet

Physical Connections

SV5C-EDP ANALYZER

The physical connections of the SV5C-eDP Analyzer are shown in Figure 2. The required pinout for the MXP connector of the SV5C-eDP Analyzer is shown in Table 2 below.

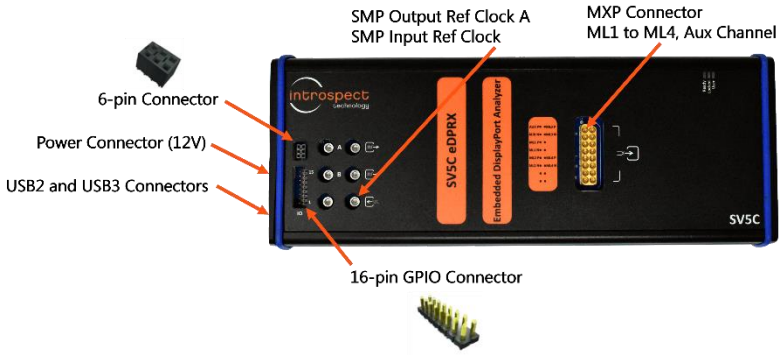


Figure 2: SV5C-eDP Analyzer physical connections.

TABLE 2: MXP CONNECTOR PINOUT

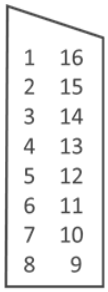
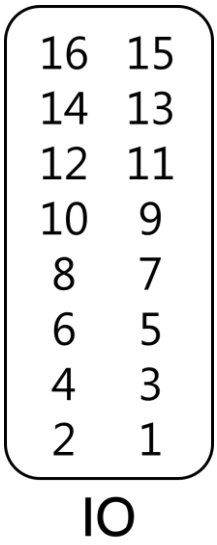
CONNECTOR	PIN	LANE
	1 2	Auxiliary Channel P Auxiliary Channel N
	3 4	ML Lane 1P ML Lane 1N
	5 6	ML Lane 2P ML Lane 2N
	16 15	ML Lane 3P ML Lane 3N
	12 11	ML Lane 4P ML Lane 4N

TABLE 3: IO CONNECTOR PINOUT

CONNECTOR	PIN	SIGNAL NAME
	1	HPD 1.2V Out
	2	User IO 1
	3	HPD 3.3V Out / HPD From Programmable DAC In
	4	User IO 2
	5	Ground
	6	Capture Triggered Out
	7	Not Connected
	8	Capture Triggered In
	9	Ground
	10	Firmware Rest In. Active-low
	11	Not Connected
	12	User I2C SCL IO
	13	Not Connected
	14	User I2C SDA IO
	15	Not Connected
	16	HPD 1.8V Out / HPD 1.8V In

CONNECTING THE SV5C-EDP TO A DEVICE UNDER TEST

OPTION 1: DIRECT CONNECTION WITH COAXIAL CABLES

The diagram in Figure 3 below illustrates the direct connection of the SV5C-eDP Analyzer to a device under test via coaxial cables. The recommended cable part numbers for this type of connection are provided below.

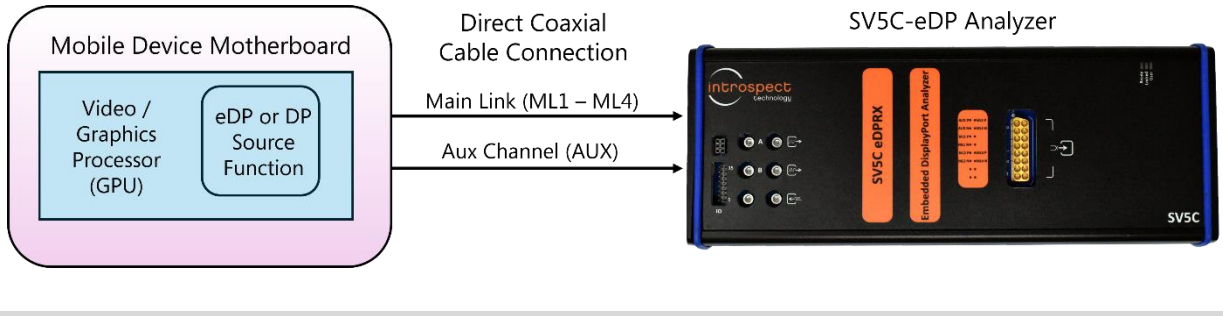


Figure 3: Illustration of direct connection to the SV5C-eDP Analyzer via coaxial cables.

DisplayPort Plug Adapter: Plug to SMA Male

Wilder Technologies DP-TPA-P, Part Number 640-0001-000

MXP Cable Harness: SMA Female to MXP

Huber and Suhner, MF53/2x8A_21MXP/21SMA/152

OPTION 2: ACTIVE PROBING OF A DISPLAYPORT BUS

The diagram in Figure 4 on the following page illustrates a bus probing application using the Introspect PV2 Universal Active Probes. Photos of each of the elements of the PV2 probing solution are shown in further detail in Figure 5.

An example of this probing option is also provided in Figure 16 in the "Example Application" section of this document.

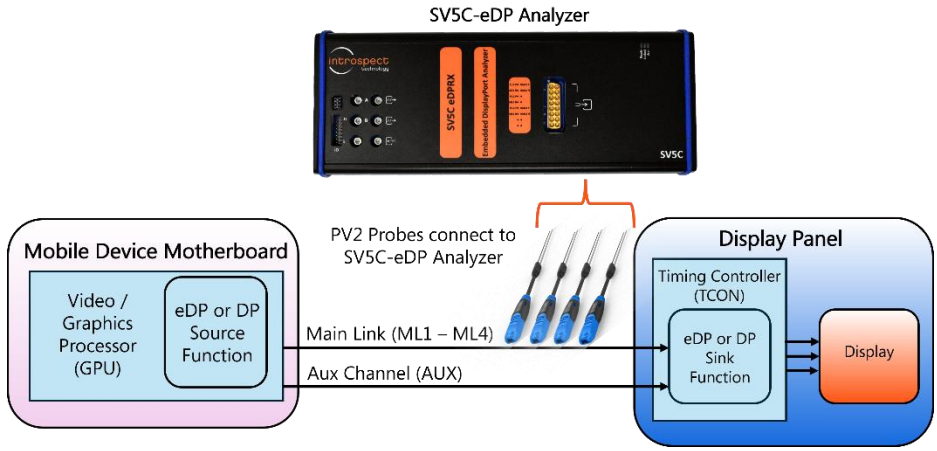


Figure 4: Illustration of an SV5C-eDP Analyzer application which uses PV2 probes.

The part numbers for this type of connection are provided below.

PV2 Universal Active Probe: Probe Tip on bus to SMA Male, Introspect Part Number 7154

PV2PSU PV2 Power Supply: Introspect Part Number 7155

MXP Cable Harness: SMA Female to MXP

Huber and Suhner, MF53/2x8A_21MXP/21SMA/152

Please refer to "Ordering Information" and "Additional Documentation" listed in the previous section of this document for further information on the PV2 probe solution.

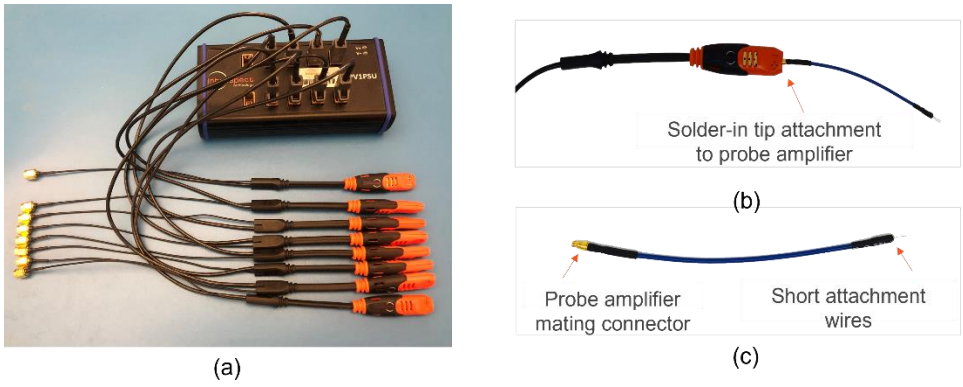


Figure 5: (a) PV2 probe solution for DisplayPort applications: (b) PV2 probe amplifier (c) PV2 solder-in tip.

OPTION 3: PROBING A DISPLAYPORT BUS WITH A CHASSIS PROBE

For (non-embedded) DisplayPort bus probing applications where connector configurations preclude soldering PV2 probes directly onto a bus, a DisplayPort fanout device can be used. The system block diagram is illustrated in Figure 6 below. The part numbers for this type of connection are:

DisplayPort 1:2 Fanout Chassis Probe: Introspect Part Number 6312 or 6313

MXP Cable Harness: SMA Female to MXP

Huber and Suhner, MF53/2x8A_21MXP/21SMA/152

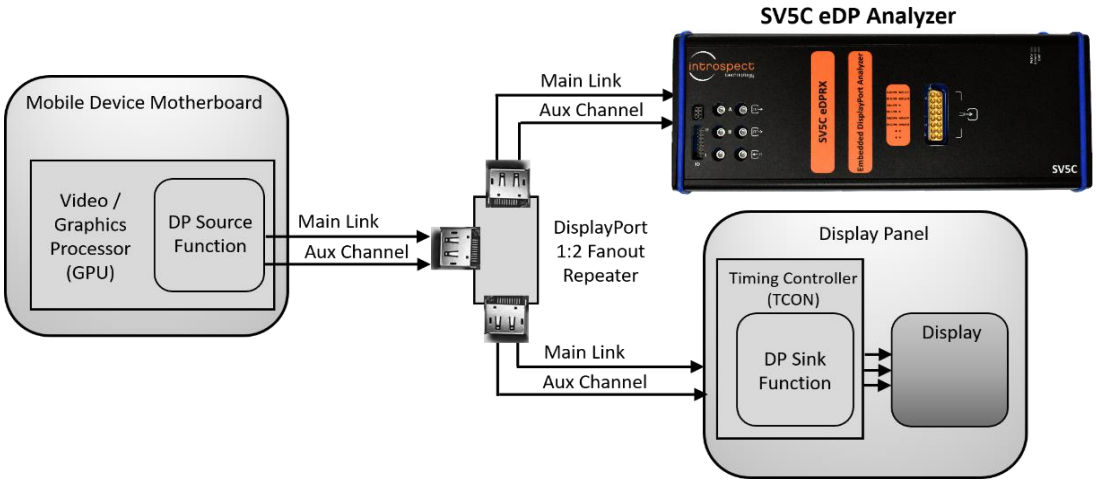


Figure 6: Illustration of SV5C-eDP Analyzer with a chassis probe device for Display Port bus probing applications.

NOTE

Option 3 is intended for systems where a physical DisplayPort connector is required. For Embedded DisplayPort applications, please see Option 4 below.

OPTION 4: REMOTE SAMPLING HEAD FOR EMBEDDED DISPLAYPORT SYSTEMS

The Introspect Remote Sampling Head is ideal for Embedded DisplayPort IC probing applications such as Device Driver Integrated Circuits (DDIC) probing or Embedded DisplayPort bus probing, each without external DisplayPort cables. A diagram of a typical application and each of the elements of the test solution are shown in Figure 7 below. The customer provides the flex cable and flex cable attachment to the board under test. The part numbers for this type of connection are:

RSH2 Remote Sampling Head: Introspect Part Number 7104

MXP Cable Harness: MXP to MXP

Part Number: Huber and Suhner MF53/2x8A_21MXP/21MXP/305_1

Please refer to "Ordering Information" and "Additional Documentation" listed in the previous section of this document for further information on Remote Sampling Head solutions.

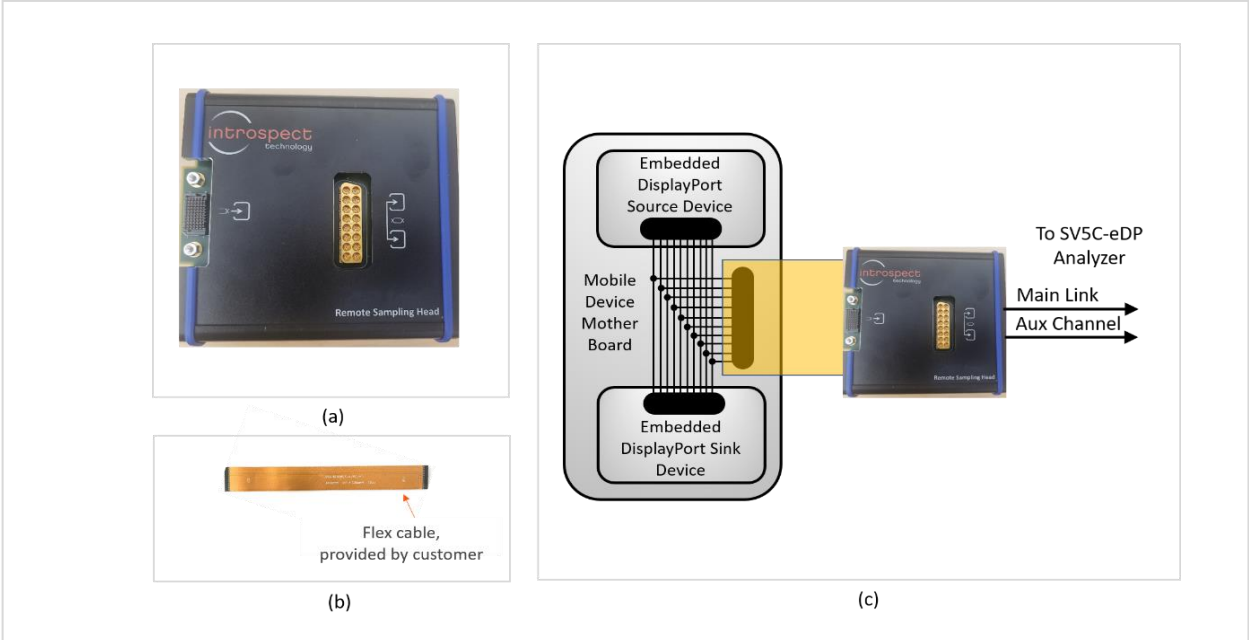


Figure 7: (a) Photo of the Remote Sampling Head for Embedded DisplayPort Applications (b) Flex cable from customer DUT (c) Typical application where Remote Sampling Head provides a compact probing solution.

In summary, Introspect Technology fully supports each of the four connection options. Pinetree is automatically compatible with each of the above cases.

Detailed Feature Description

THE PINETREE ENVIRONMENT

The SV5C-eDP Analyzer is operated using Introspect's award-winning software, Pinetree, which is a Python-based scripting environment. It includes a comprehensive suite of components and methods for test automation and full analysis of Embedded DisplayPort systems.

Figure 8 below shows the main windowpanes for setting up a test. The bottom windowpane contains the main "Test Procedure". The test procedure is a Python script referred to as "Components". The windowpane on the top left contains the pre-built or custom Components. The windowpane on the top right contains the "Properties" associated with each Component.

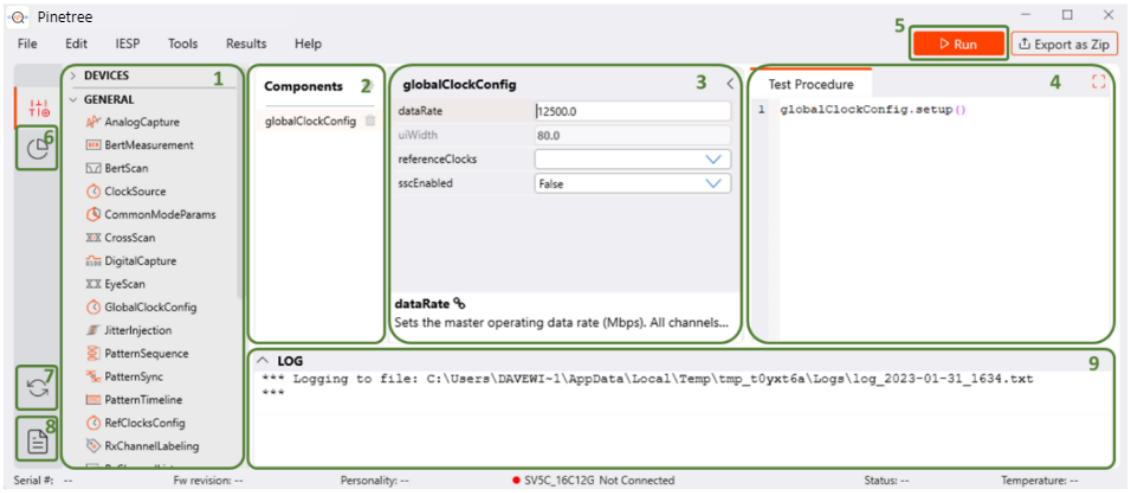


Figure 8: Main test window

1. Create new component tray (double click or drag in 2.)
2. Component list
3. Component properties panel
4. Procedure python code editor
5. Run button: start the current test
6. Result tray
7. Firmware updater
8. Link to form factor documentation (opens in web browser)
9. Application log

LANE AND DATA RATE CONFIGURATION

Figure 9 below shows Pinetree's components which configure the lane and data rates of the SV5C-eDP Analyzer, as highlighted in red.

The Analyzer may be configured to 1, 2 or 4 lanes (ML1 to ML4) for DisplayPort or configured to any number of lanes up to 4 for custom Embedded DisplayPort applications.

Data rates may be configured in a continuous range from 80 Mbps to 10.1 Gbps, providing coverage for protocols for DisplayPort v2.1 and Embedded DisplayPort v2.0. See Table 4 in the Specifications section of this document for details on direct connect mode and bus probe mode.

Figure 9: Examples of configuring data rate and lane list in the Pinetree software.

STREAM ATTRIBUTES AND IMAGE FORMATS

Figure 10 shows the Pinetree component which configures the stream attributes the SV5C-eDP Analyzer is expected to receive. Both enhanced data framing mode and data descrambling are supported by the analyzer, and the scrambling seed is configurable through the Pinetree GUI.

The analyzer provides full decoding for RGB, YCbCr and Display Stream Compression (DSC) pixel formats. The number of streamed lanes for analysis may be specified differently than the number of lanes defined in the lane list to make most efficient use of the capture memory.

See Table 5 in the Specifications section of this document for the complete listing of stream attributes supported.

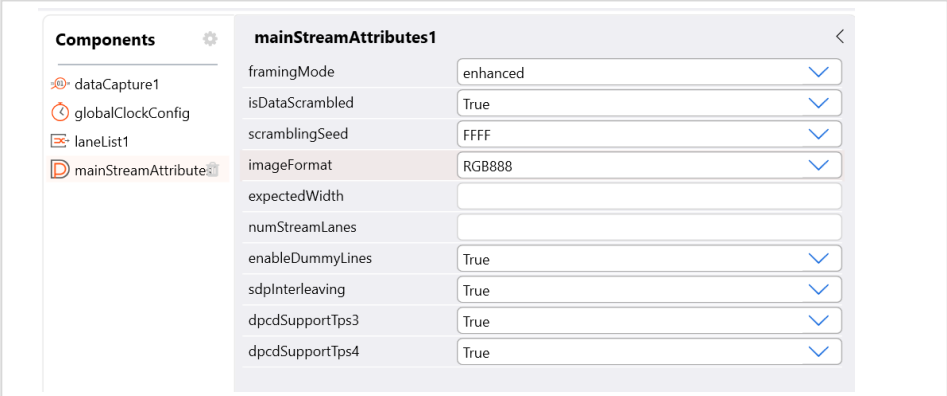


Figure 10: Examples of configuring frame attributes in Pinetree.

CAPTURE CONFIGURATION

Figure 11 shows the Pinetree component for configuring a data capture. The transport mode can be configured to Single-Stream Transport (SST), Multi-SST Operation (MSO), 8b10b Multi-Stream Transport (MST) or 128b132b MST. The SV5C-eDP triggers the start of a data capture based on user-configurable trigger conditions. The list of available conditions includes, amongst many others, the scrambler reset, frame start, blanking start, user-defined SDPs and AUX commands.

The SV5C-eDP ends a capture based on a set of user-configurable conditions as listed in "postTriggerType" in the figure. Types of data capture post-triggers include durations measured in time, in symbols, or in number of frames. For a complete list of supported trigger conditions and post-trigger types, please refer to Table 5 in the "Specifications" section of this document.

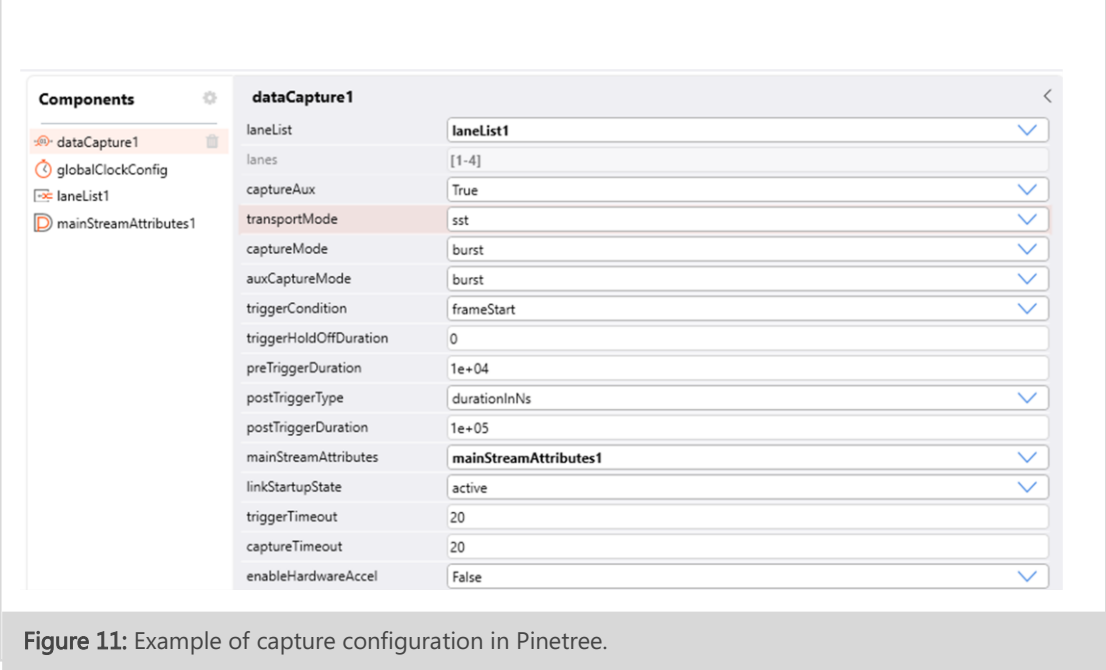


Figure 11: Example of capture configuration in Pinetree.

PINETREE DATA CAPTURE VIEWERS

All data captured by the SV5C-eDP Analyzer is accessible in terms of raw bytes on a per lane basis. The analyzer decodes symbols, detects display parameters, and automatically extracts video frames. Built-in viewers are provided for easy visual analysis and data collection.

Figure 12 shows an example of the Pinetree data capture viewer displaying the capture summary, timestamps, and reconstructed frames. Data capture viewers also provide hyperlinks between frames, packets, and events, and provide detailed error reporting by error type. Pixel errors, symbol errors, and dummy / fill errors are detected by the data capture tool.

Packet viewers also provide the ability to view data by lane and the ability to view traffic on the main link correlated with the Auxiliary Channel events.

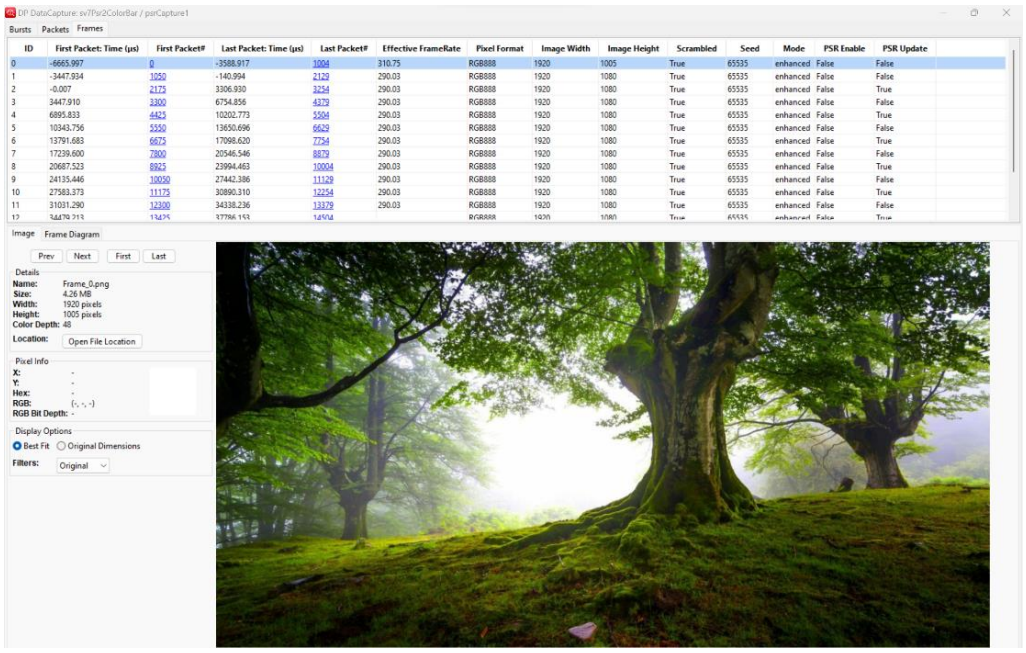


Figure 12: Example of the Pinetree data capture viewer, Frames tab.

DETAILED CAPTURE TABLES: DATA, EVENTS AND SYMBOLS

All data captured by the SV5C-eDP Analyzer is accessible for post-processing within the powerful Python scripting environment of the Pinetree GUI. With Python component-level documentation and with several fully coded examples, a user can rapidly retrieve detailed tables for data, events, or symbols.

Figure 13 illustrates a portion of a typical Event Table that is generated in Pinetree. For reference, the right side of the figure shows the DisplayPort Video stream construction according to the Embedded DisplayPort specification. In the Event Table on the left side of the figure, the Line Data, Blanking Start and End, Line Footers, and Dummy (or Audio) Data and received symbols are all tabulated by Pinetree for easy visual analysis.

Figure 14 provides an example of a Symbol Table generated in Pinetree. Symbols are highlighted and are traceable by index or lane.

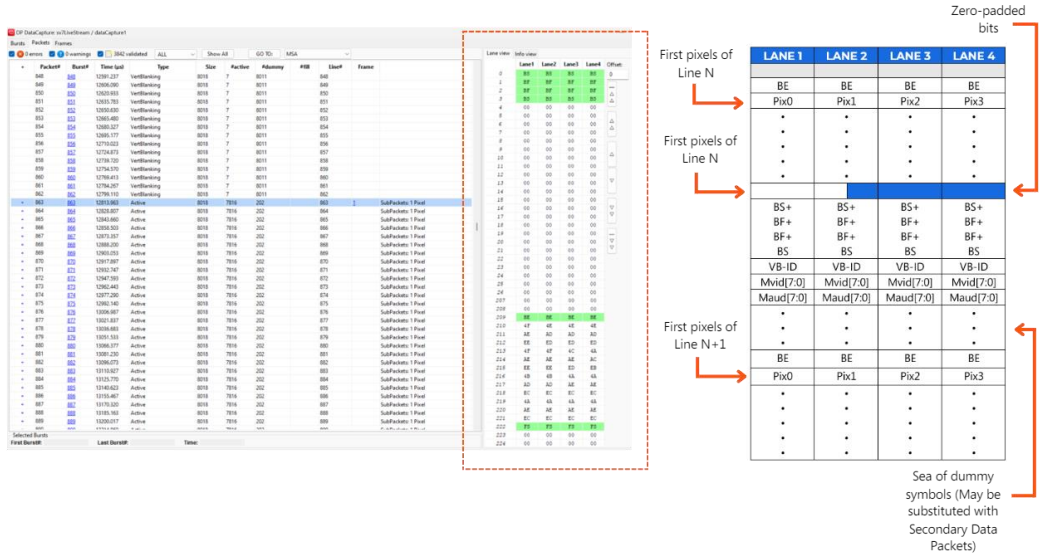


Figure 13: Example of a typical Event Table generated in Pinetree.

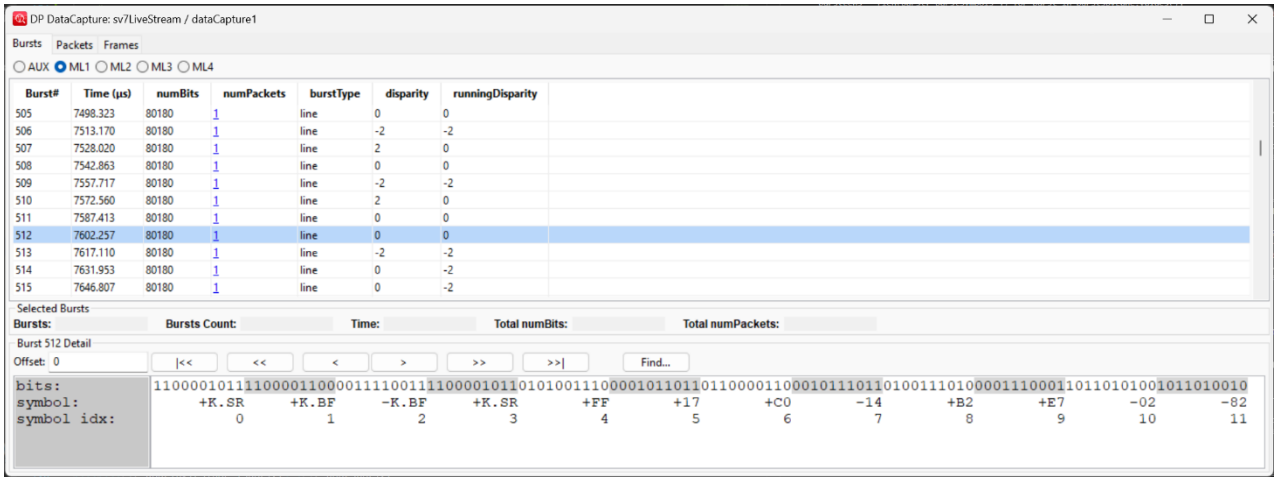


Figure 14: Example of a typical Symbol Table generated in Pinetree.

Example Application

EDP BUS PROBING WITH THE SV5C-EDP ANALYZER

A typical target application is probing of an Embedded DisplayPort bus. A high-level diagram of the test setup is as shown below in Figure 15. The following section will provide an overview of hardware and software requirements and hardware setup for this application.

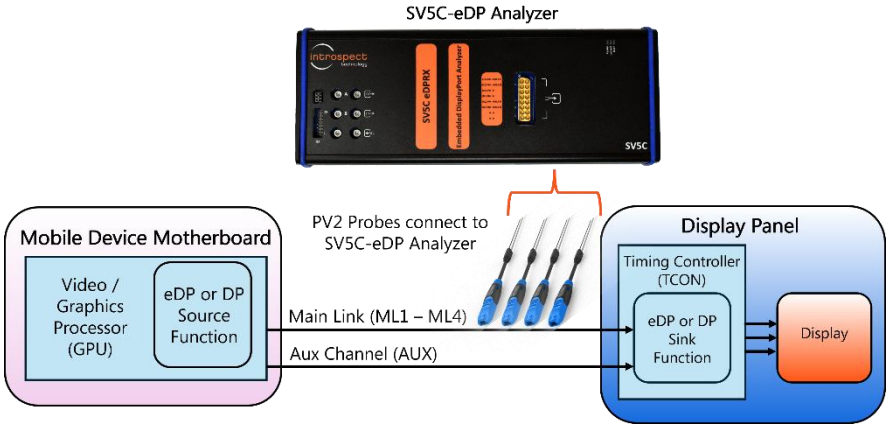


Figure 15: Typical application of the SV5C-eDP Analyzer and PV2 Probes connected to an Embedded DisplayPort system.

HARDWARE REQUIREMENTS

The full list of hardware required for the SV5C-eDP bus probing solution is given below:

- (QTY = 1) DisplayPort source (e.g., PC) and Sink device (PC monitor) as a system under test.
- (QTY = 1) SV5C-eDP Analyzer
- (QTY = 1) PV2PSU Probe Power Supply
- (QTY = 2) 12V DC Voltage Adapter (included with Analyzer and PV2PSU Power Supply)
- (QTY = 8) PV2 Active Probes, for connection to eDP lanes ML1 (P/N) to ML4 (P/N)
- (QTY = 8) Solder-Down Probe Tips, for connection to DisplayPort bus breakout board.
- (QTY = 2) Standard DisplayPort cables, for connection to DisplayPort Source to breakout board and breakout board to DisplayPort Sink.

- (QTY = 1) MXP to SMA Cable Assembly (included with Analyzer)
- A PC connected to the SV5C-eDP Analyzer via a USB2.0 mini B and USB3.0 micro B cable, for controlling Pinetree. See software requirements below.

SOFTWARE SYSTEM REQUIREMENTS

To run Pinetree, the following are required:

- A PC installed with Windows 10 or later
- The Pinetree install executable at version 24.3.0 or later
- SV5C-eDP Analyzer firmware at version FWSV5CEDPRX01A001 or later

NOTE

A fully functional command line version of Pinetree is also available for MacOS and Linux.

HARDWARE SETUP

An example of the interconnection of the SV5C-eDP, the PV2 probes and PV2PSU power supply is shown below in Figure 16(a). For illustrative purposes, PV2 probes are shown connected to a breakout board for a DisplayPort Bus in Figure 16(b). The full setup is driving a PC monitor, as in Figure 16(c).

Any combination of the four DisplayPort lanes (ML1 to ML4) may be connected to the SV5C-eDP.

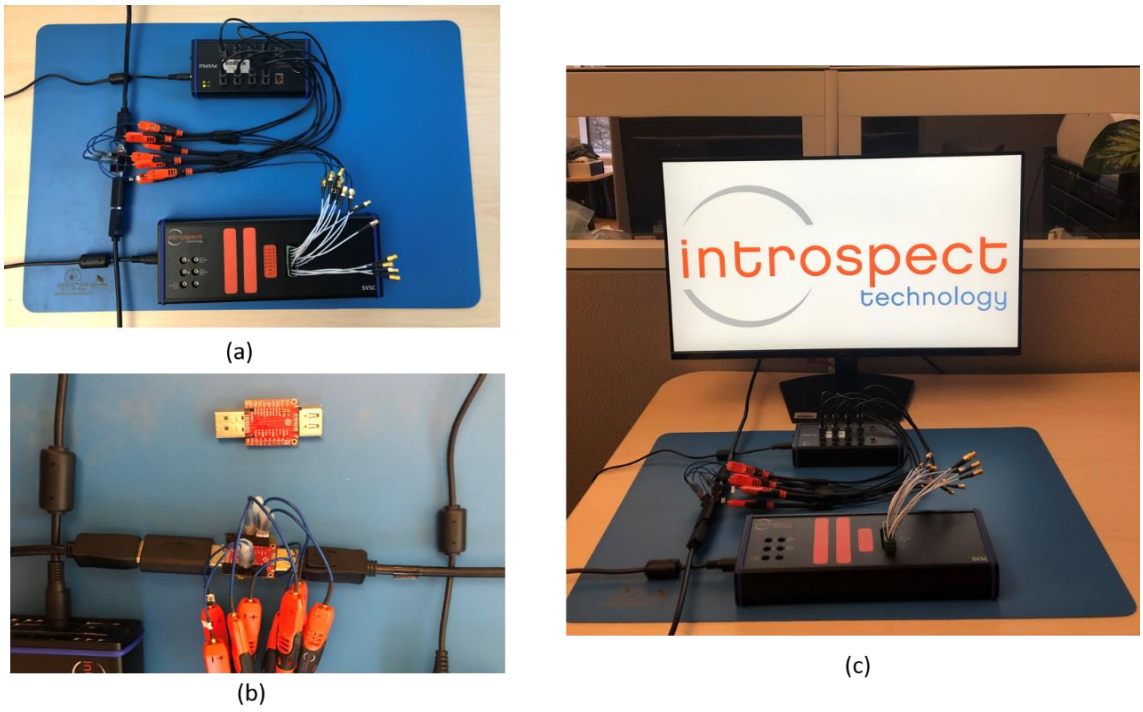


Figure 16: (a) Connection of SV5C-eDP Analyzer, PV2 probes / PV2PSU power supply, to a DisplayPort bus (b) Close-up of probe connection DisplayPort bus, including DisplayPort bus breakout board (c) Complete setup, including the live PC monitor with the stream being analyzed.

Specifications

TABLE 4: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol			
Physical Layer Interface	eDP DP		Support for eDP to version 2.0 Support for DP to version 2.1
Ports			
Number of Analyzer Lanes	5		ML1 to ML4 Aux Channel (bidirectional)
Number of GPIO pins	2		Programmable as external trigger input or flag output pins
Number of dedicated reference clock inputs	1		
Number of dedicated reference clock outputs	2		
PC connections for Pinetree Control	2		USB2 and USB3
Data Rates and Reference Clocks			
Minimum Data Rate	80	Mbps	Per Lane
Maximum Data Rate	10.1	Gbps	Per Lane
Minimum External Input Ref Clock	10	MHz	
Maximum External Input Ref Clock	250	MHz	
Minimum External Output Ref Clock	10	MHz	
Maximum External Output Ref Clock	500	MHz	
Power Consumption			
DC Input Voltage	12	V	
Power Dissipation	80	W	

TABLE 5: EDP RECEIVER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Input Voltage and Equalization			
Minimum detectable differential voltage, |VID|	90	mV	Measured at SV5C MXP connector
Maximum allowable differential voltage, |VID|	900	mV	Measured at SV5C MXP connector
Programmable range for differential threshold voltage	+/- 400	mV	
Minimum Equalization DC Gain	0	dB	
Maximum Equalization DC Gain	8	dB	
Direct Connection: Receiver Lane Input Coupling			
Single-Ended Input Impedance	50	Ohm	Impedance seen by DisplayPort Source Direct MXP connection
Single-Ended Input Impedance Tolerance	+/- 5	Ohm	Impedance seen by DisplayPort Source Direct MXP connection
Maximum Data Rate	10.1	Gbps	Direct Connection
PV2 Connection: Receiver Lane Coupling to Bus			
Single Ended Bus Loading	600	Ohm	Per Wire on eDP or DP bus (see Figure 15 and Figure 16)
Maximum Data Rate	10.1	Gbps	PV2 Probe Connection (see Figure 15 and Figure 16).

TABLE 6: DATA CAPUTRE AND ANALYSIS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Features			
Frame Modes	Standard Enhanced		
Supported Pixel Formats	RGB YCbCr		RGB666, RGB888, RGB999, RGB101010, RGB111111, RGB121212, RGB161616 YCbCr422, YCbCr444 and Y-Only at: 6-bit, 8-bit, 9-bit, 10-bit, 11-bit, 12-bit and 16-bit
Supported YCbCr Standard	YCbCr601 YCbCr709		
Data Scrambling Support	Yes		
Scrambling Seeds	DP eDP		
Display Stream Decompression (DSC) Support	Yes		
Forward Error Correction (FEC) Support	Yes		
Trigger Conditions for Data Capture			Immediate, or as defined by: Scrambler Reset Blanking Start / End Fill Start / End Frame Start PHY Sleep, PHY Standby AUX-Wake ML Symbol Alignment User-defined Control Symbol User-defined Secondary Packet (Header, Payload or both) User-defined AUX Command External Trigger

Specification of Data Capture Duration			Defined by: Duration in time (ns) Duration in symbols Number of frames Next frame or next Blanking End
Memory Depth	8	GByte	Max captured ML data per lane: 1 GB with 3 or less ML lanes 0.5 GB with 4 ML lanes

TABLE 7: PHYSICAL CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Dimensions			
Length	11.2, 285	in, mm	
Width	4.25, 108	in, mm	
Height	1.7, 43	in, mm	
Weight	3	lbs	
Physical Connections			
ML1 to ML4, Aux Channel	MXP		Huber & Suhner, 16 pin
IO Connector			Available through 16 pin header IO Connector 15-91-2125
Ref Clock In	SMP		SMP Differential Pair
Ref Clock Out	SMP		SMP Differential Pair
PC connection	USB2 USB3		USB2.0 mini B USB3.0 micro B
Power Switch / Connector			AC adapter provided 110/220 V, 50/60 Hz

Revision Number	History	Date
1.0	Document Release	November 24, 2020
1.1	Added detailed feature descriptions	December 10, 2020
1.2	Updated pinout, updated information on PV2 solutions, and revised specifications including maximum data rate	April 12, 2022
1.3	Updated: the Molex GPIO pinout, all software GUI screenshots, DP & eDP supported versions, and probe item numbers	June 12, 2023
1.4	Updated the IO Connector pinout; text, figures.	August 22, 2024

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Published in Canada on August 22, 2024
EN-D027E-E-24235

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