



DATASHEET

SV7C-eDP Analyzer

Embedded DisplayPort Analyzer

C SERIES

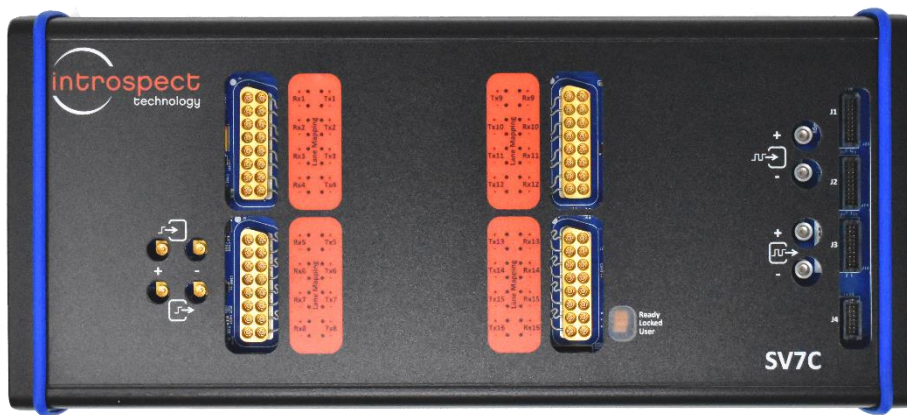


Table of Contents

Introduction	3
Overview	3
Key Features	3
Ordering Information.....	4
Additional Documentation	4
Physical Connections	5
SV7C-eDP Analyzer.....	5
MXP Main Link Connector	5
MXP Auxiliary Channel Connector.....	6
Connecting the SV7C-eDP to a Device Under Test.....	7
Specifications	11

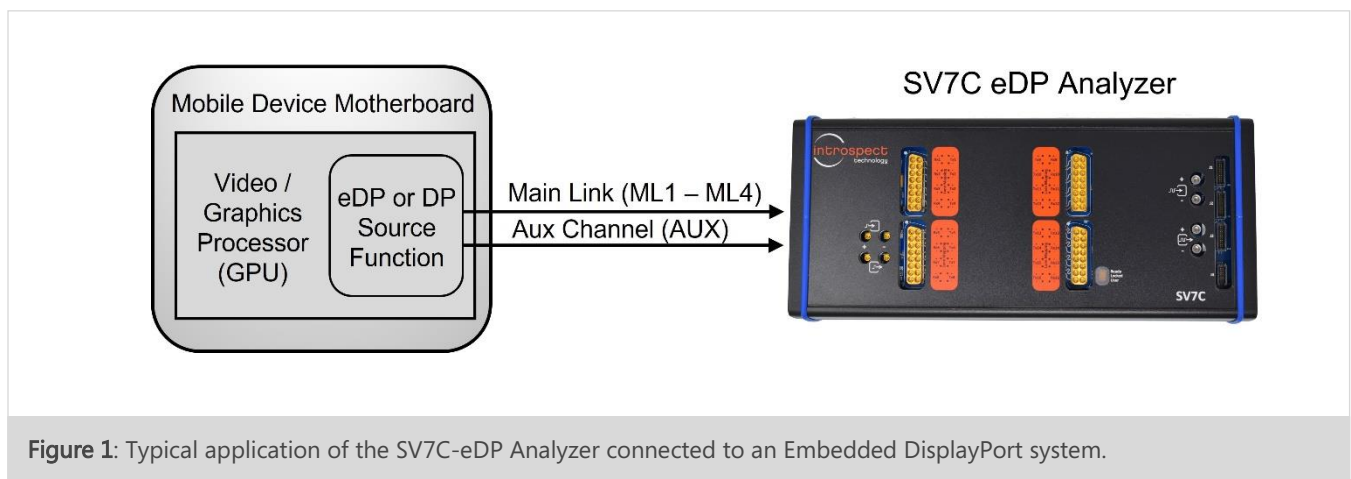
Introduction

OVERVIEW

The SV7C-eDP Embedded DisplayPort Analyzer is an ultra-portable, high-performance instrument capable of analyzing traffic for Embedded DisplayPort and DisplayPort applications. The SV7C-eDP Analyzer may be used as either a DisplayPort sink device (for source testing) or as a probing solution for capturing protocol traffic on an Embedded DisplayPort bus. The Analyzer detects display parameters, supports link training, captures live traffic, and extracts full video frames. All these functions are integrated into the award-winning Pinetree™ software environment. Figure 1 below illustrates a typical application of the SV7C-eDP Analyzer connected to an Embedded DisplayPort Source.

KEY FEATURES

- **Protocol:** supports Embedded DisplayPort (eDP) up to v2.0 and DisplayPort (DP) up to v2.1
- **Supported Data Rates:** up to 26 Gbps, including bus probing applications with Introspect PV2 active probes
- **Lane Count:** configurable from 1 to 4 lanes (ML1 to ML4) plus auxiliary channel (AUX)
- **Data Capture:** extensive triggering functions and consecutive frame capture capabilities
- **Diagnostics:** full video frame extraction and data analysis tools



ORDERING INFORMATION

TABLE 1: ITEM NUMBERS FOR THE SV7C-EDP ANALYZER WITH RELATED PRODUCTS

PART NUMBER	NAME	KEY DIFFERENTIATORS
5942	SV7C-eDP Analyzer (includes Pinetree™ software license)	High performance eDP protocol analyzer and source tester
7154	PV2 Universal 8 GHz Universal Active Probe	8 GHz active probe that is compatible with any 50 Ohm instrument
7155	PV2PSU PV2 Power Supply Unit	Power supply for PV2
6312	DisplayPort Chassis Probe with Type-C Interface (Includes Sensing Probe)	Connectorized passive chassis probe with a fanout path. The fanout path is completely transparent to main link equalization.

ADDITIONAL DOCUMENTATION

PV2 Universal Active Probe Datasheet

- MK-D035E-E-21271 PV2 8 GHz Active Probe Data Sheet

DisplayPort Chassis Probe Quick Start Manual

- EN-G059E-E-22027 DisplayPort Chassis Probe Quick Start Manual

Physical Connections

SV7C-EDP ANALYZER

The physical connections of the SV7C-eDP Analyzer are shown in Figure 2.




Figure 2: SV7C-eDP Analyzer physical connections.

MXP MAIN LINK CONNECTOR

The Main Link signals are located on the upper left MXP connector as shown in Figure 2 above and the full pinout description as given in Table 2 below.

TABLE 2: UPPER MXP CONNECTOR PINOUT

CONNECTOR	PIN	SV7C LABEL	EDP LANE
	1	Rx1+	ML Lane 1P
	2	Rx1-	ML Lane 1N
	3	Rx2+	ML Lane 2P
	4	Rx2-	ML Lane 2N
	5	Rx3+	ML Lane 3P
	6	Rx3-	ML Lane 3N
	7	Rx4+	ML Lane 4P
	8	Rx4-	ML Lane 4N

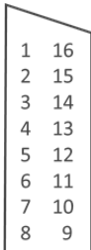
MXP AUXILIARY CHANNEL CONNECTOR

The Auxiliary Channel signals are located on the lower left MXP connector as shown in Figure 2 on the previous page and the full pinout description is given in Table 3 below.

Note that the Auxiliary Channel in DisplayPort is bi-directional, and as such there are separate MXP connections for the TX signal (the analyzer / sink controls the Auxiliary Channel) and the RX signal (the analyzer / sink receives from the Auxiliary Channel).

The connection between the TX and RX can be made externally though a combiner circuit. The recommended part for this function is Mini-Circuits ZFRSC-42-S+. The required connections between the eDP or DP source, the combiner, and the SV7C-eDP are outlined in the diagram of Figure 3.

TABLE 3: AUXILIARY CHANNEL MXP CONNECTOR PINOUT

CONNECTOR	PIN	SV7C LABEL	LANE
	16	Tx5+	Auxiliary Channel P, TX
	15	Tx5-	Auxiliary Channel N, TX
	1	Rx5+	Auxiliary Channel P, RX
	2	Rx5-	Auxiliary Channel N, RX

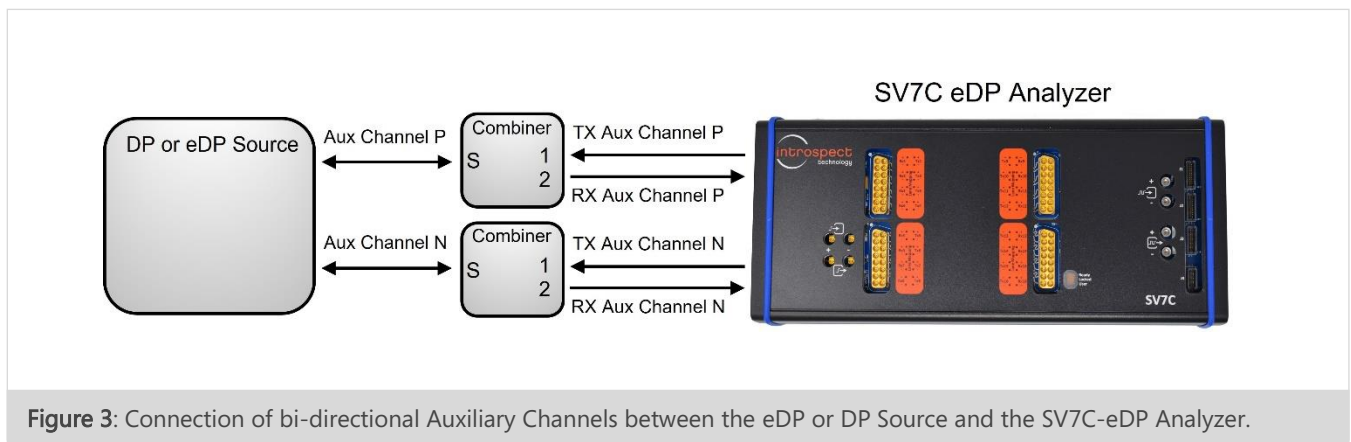


Figure 3: Connection of bi-directional Auxiliary Channels between the eDP or DP Source and the SV7C-eDP Analyzer.

CONNECTING THE SV7C-EDP TO A DEVICE UNDER TEST

OPTION 1: DIRECT CONNECTION WITH COAXIAL CABLES

The diagram in Figure 4 below illustrates the direct connection of the SV7C-eDP Analyzer to a device under test via coaxial cables. The recommended cable part numbers for this type of connection are provided below.

DisplayPort Plug Adapter: (a) Plug to SMA Female or (b) USB Type-C to SMA Female

(a) Wilder Technologies DP-TPA-P, Part Number 640-0001-000

(b) Wilder Technologies DPC-TPA-P, Part Number 640-0800-000

MXP Cable Harness: SMA Male to MXP or SMA Female to MXP

Huber and Suhner, MF53/2x8A_21MXP/11SK/305, Introspect Part Number 4810 or

Huber and Suhner, MF53/2x8A_21MXP/21SMA/152, Introspect Part Number 4813

The shorter 6" cable length is preferable for higher bandwidth applications.

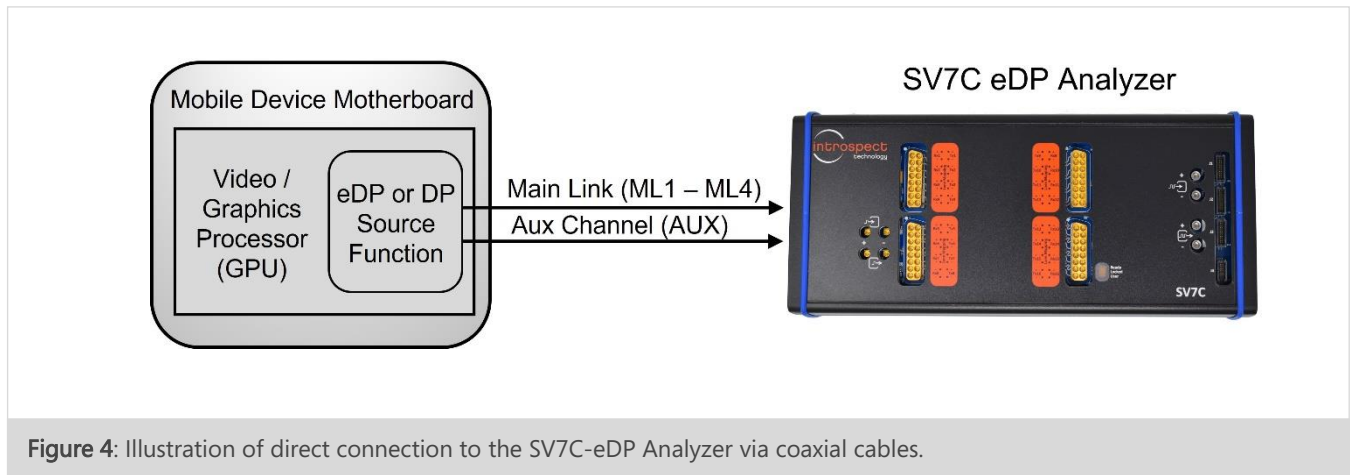


Figure 4: Illustration of direct connection to the SV7C-eDP Analyzer via coaxial cables.

OPTION 2: ACTIVE PROBING OF A DISPLAYPORT BUS

The diagram in Figure 5 on the following page illustrates a bus probing application using the Introspect PV2 Universal Active Probes. Photos of each of the elements of the PV2 probing solution are shown in further detail in Figure 6.

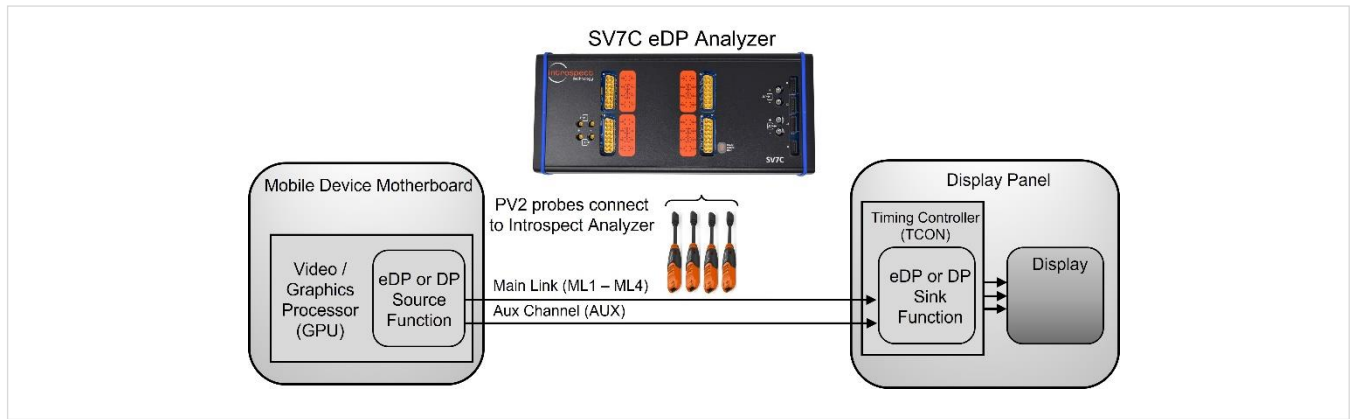


Figure 5: Illustration of an SV7C-eDP Analyzer application which uses PV2 probes.

The part numbers for this type of connection are provided below.

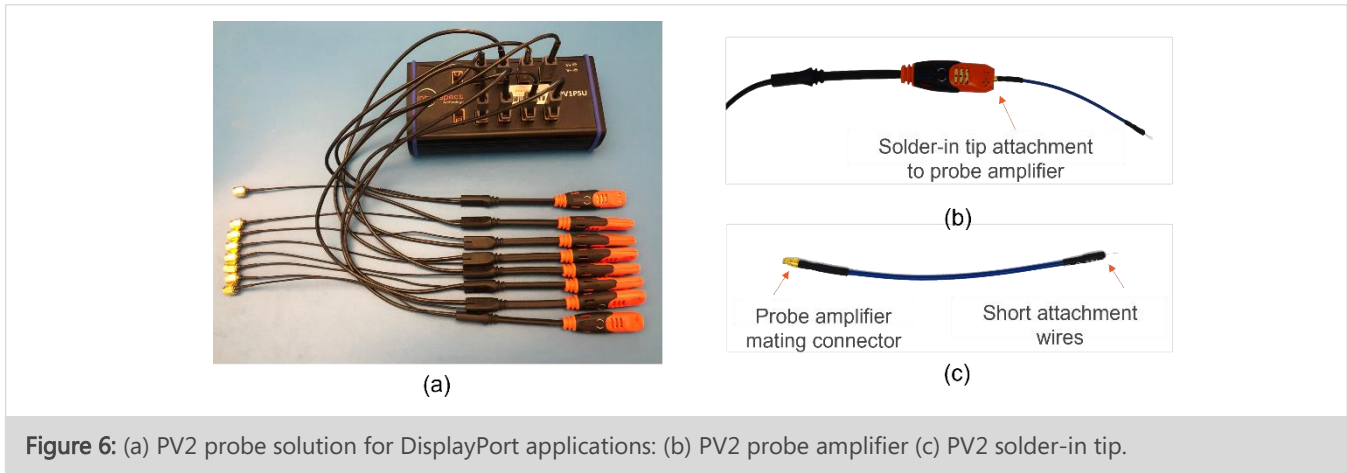
PV2 Universal Active Probe: Probe Tip on bus to SMA Male, Introspect Part Number 7154

PV2PSU PV2 Power Supply: Introspect Part Number 7155

MXP Cable Harness: SMA Female to MXP

Huber and Suhner, MF53/2x8A_21MXP/21SMA/152, Introspect Part Number 4813

Please refer to “Ordering Information” and “Additional Documentation” listed in the previous section of this document for further information on the PV2 probe solution.



OPTION 3: PROBING A DISPLAYPORT BUS WITH A CHASSIS PROBE

For (non-embedded) DisplayPort bus probing applications where connector configurations preclude soldering PV2 probes directly onto a bus, a DisplayPort fanout device can be used. The system block diagram is illustrated in Figure 7 below. The part numbers for this type of connection are:

DisplayPort Chassis Probe: Introspect Part Number 6312 or 6313

MXP Cable Harness: SMA Female to MXP

Huber and Suhner, MF53/2x8A_21MXP/21SMA/152

NOTE

Option 3 is intended for systems where a physical DisplayPort connector is required.

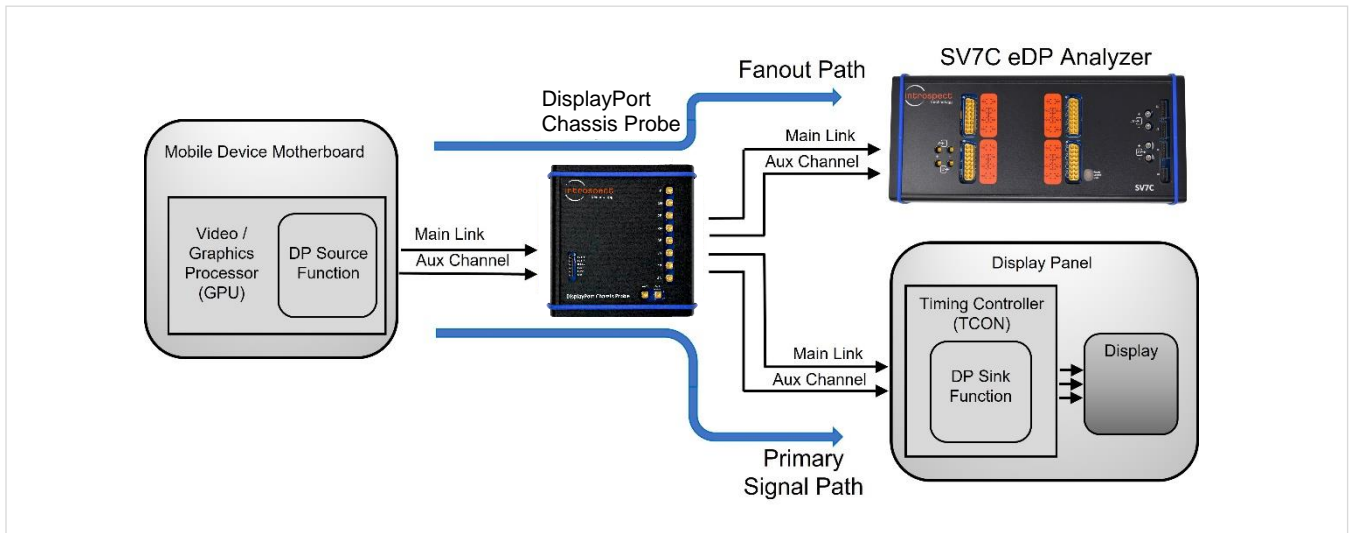


Figure 7: Illustration of SV7C-eDP Analyzer with a DisplayPort Chassis Probe device for DisplayPort bus probing applications.

In summary, Introspect Technology fully supports each of the three connection options. The Pinetree™ software is automatically compatible with each of the above cases.

Specifications

TABLE 4: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol			
Physical Layer Interface	eDP DP		Support for eDP to version 2.0 Support for DP to version 2.1
Ports			
Number of Analyzer Lanes	5		ML1 to ML4 Aux Channel (bidirectional)
Number of GPIO pins	30		Programmable as external trigger input or flag output pins
Number of dedicated reference clock inputs	1		
Number of dedicated reference clock outputs	1		
PC connections for Pinetree™ Software Control	2		USB2 and USB3 Type-C
Data Rates and Reference Clocks			
Minimum Data Rate	1.0	Gbps	Per Lane
Maximum Data Rate	26	Gbps	Per Lane
Minimum External Input Ref Clock	10	MHz	
Maximum External Input Ref Clock	250	MHz	
Minimum External Output Ref Clock	10	MHz	
Maximum External Output Ref Clock	500	MHz	
Power Consumption			
DC Input Voltage	12	V	
Power Dissipation	TBD	W	

TABLE 5: EDP RECEIVER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Input Voltage and Equalization			
Minimum detectable differential voltage, $ V_{ID} $	90	mV	Measured at SV7C MXP connector
Maximum allowable differential voltage, $ V_{ID} $	900	mV	Measured at SV7C MXP connector
Programmable range for differential threshold voltage	+/- 400	mV	
Minimum Equalization DC Gain	0	dB	
Maximum Equalization DC Gain	8	dB	
Direct Connection: Receiver Lane Input Coupling			
Single-Ended Input Impedance	50	Ohm	Impedance seen by DisplayPort Source Direct MXP connection
Single-Ended Input Impedance Tolerance	+/- 5	Ohm	Impedance seen by DisplayPort Source Direct MXP connection
Maximum Data Rate	26	Gbps	Direct Connection
PV2 Connection: Receiver Lane Coupling to Bus			
Single Ended Bus Loading	600	Ohm	Per Wire on eDP or DP bus
Maximum Data Rate	10	Gbps	PV2 Probe Connection

TABLE 6: DATA CAPTURE AND ANALYSIS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Features			
Frame Modes	Standard Enhanced		
Supported Pixel Formats	RGB YCbCr		RGB666, RGB888, RGB999, RGB101010, RGB111111, RGB121212, RGB161616 YCbCr422, YCbCr444 and Y-Only at: 6-bit, 8-bit, 9-bit, 10-bit, 11-bit, 12-bit and 16-bit
Supported YCbCr Standard	YCbCr601 YCbCr709		
Data Scrambling Support	Yes		
Scrambling Seed	FFFE, FFFF		Up to eDP v2.0/DP v2.1
Display Stream Decompression (DSC) Support	Yes		
Forward Error Correction (FEC) Support	Yes		
Trigger Conditions for Data Capture			Immediate, or as defined by: Blanking Start, Blanking End Fill Start, Fill End Frame Start Scrambler Reset Main Link Detect, Aux Detect PHY Sleep, PHY Standby K28.5 pattern (up to eDP v2.0/DP v2.1)
Specification of Data Capture Duration			Defined by: Duration in time (ns) Duration in symbols Number of frames Next frame or next Blanking End

Memory Depth	8	GByte	For received capture data
--------------	---	-------	---------------------------

TABLE 7: PHYSICAL CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Dimensions			
Length	10.75, 273	in, mm	
Width	4.92, 125	in, mm	
Height	2.20, 56	in, mm	
Weight	5	lbs	
Physical Connections			
ML1 to ML4, Aux Channel	MXP		Huber & Suhner, 16 pin
GPIO			Available through 14 pin and 20 pin headers, with connector part numbers: Samtec TFM-107-01-X-D Samtec TFM-110-01-X-D
Ref Clock In	SMP		SMP Differential Pair
Ref Clock Out	SMP		SMP Differential Pair
PC connection	USB2 USB3		USB2.0 mini B USB3.0 Type-C
Power Switch / Connector			AC adapter provided 110/220 V, 50/60 Hz



Revision Number	History	Date
1.0	Document Release	November 2, 2022
1.2	Updated Chassis Probe terminology	December 23, 2024

The information in this document is subject to change without notice and should not be construed as a commitment by Introspect Technology. While reasonable precautions have been taken, Introspect Technology assumes no responsibility for any errors that may appear in this document.



© Introspect Technology, 2024
Published in Canada on December 23, 2024
EN-D037E-E-24358

INTROSPECT.CA