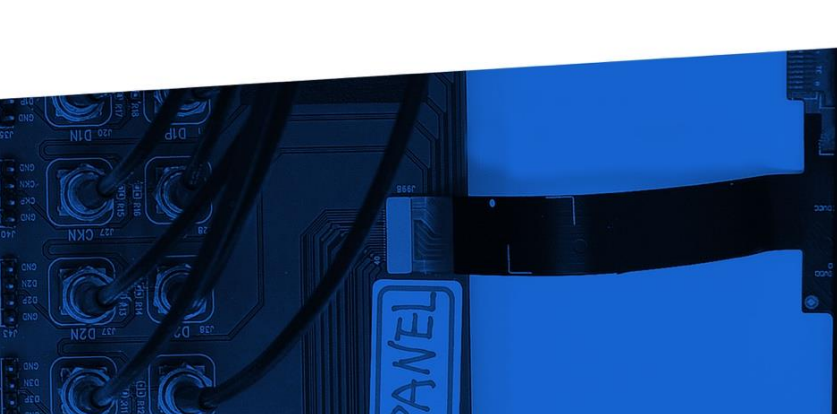
introspect technology

DATA SHEET

SV6E-X

Mid-Frequency Digital Test Module

E SERIES



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Introduction

OVERVIEW

The **SV6E-X Mid-Frequency Digital Test Module** is an all-inclusive system for designing, validating, and characterizing digital I/O interfaces that operate at frequencies up to 200 MHz. Configurable to natively support multiple protocols, this module replaces racks of equipment that are typically required for I/O AC characterization and design validation. For any given protocol, the SV6E-X contains three instrument components: a protocol exerciser with fine-resolution edge placement capability, a protocol analyzer with fine-resolution timing analysis, and a two-channel real-time oscilloscope. All three instrument components are accessible simultaneously and in real-time using the award-winning Pinetree software, thus making the SV6E-X a complete solution for popular protocols such as MIPI I3C, Quad SPI, MIPI SoundWire, JEDEC SidebandBus, SMBus, PMBus, MIPI SPMI, and many others.

FEATURES

- Two I/O banks, each containing 10 single-ended channels; channel usage depends on the licensed protocol
- 200 MHz capable I/O in hardware; the application-specific maximum operating frequency depends on the licensed protocol
- Two programmable, high-current device power supplies, one for each bank
- PurVue Analyzer™ technology available on any I/O channel
- Protocol licenses available on demand

BENEFITS

- Supports wide-bus applications such as Octal SPI
- Replaces PXI-based test systems or similar vector-based ATE
- Replaces bench oscilloscopes and associated software decoding licenses
- Supports automated and high throughput protocol-based CTS applications
- Future-proof hardware investment with a long-term protocol and support roadmap

System Components

Figure 1 shows a high-level description of the four main system components in the SV6E-X. Each protocol will typically have different quantities of these instances, but they all share the common architecture consisting of a device core (protocol exerciser), an analyzer core, a set of I/O ports, and an oscilloscope. The following subsections explain these concepts in more detail.

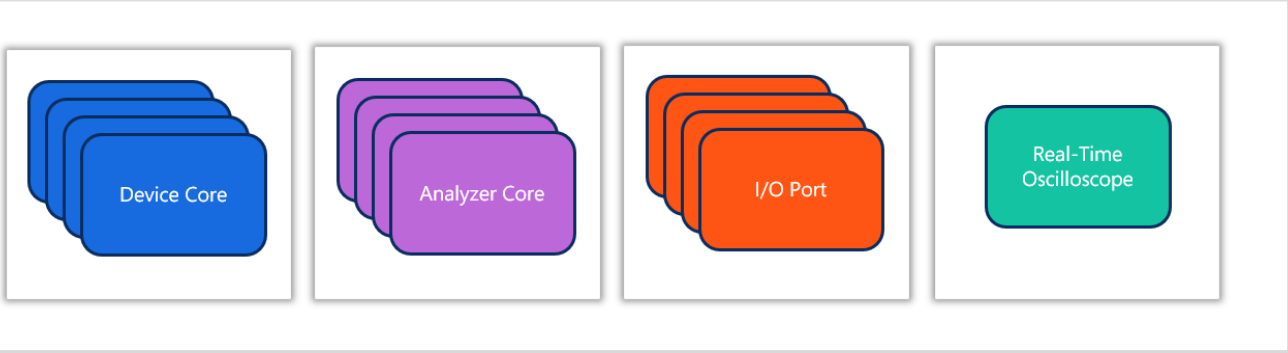


Figure 1: Four system component categories exist in the SV6E-X hardware.

DEVICE PORTS

Each SV6E-X device port consists of a grouping of I/O elements, each offering the following features:

- LVCMOS push-pull driver with 50 Ohm series termination
- Open-drain driver with a switchable open-drain pull-up resistor
- LVCMOS high-impedance receiver
- Switchable high-keeper and bus hold resistor

Each of these features is dynamically adjustable based on the protocol being deployed. For example, in I3C applications, a single I/O element will switch between open-drain and push-pull mode dynamically. Additionally, for multi-port applications or protocols that do not require high-keeper capability, each bus high-keeper resistor can be completely disabled through software. Figure 2 shows a functional representation of the I/O elements.

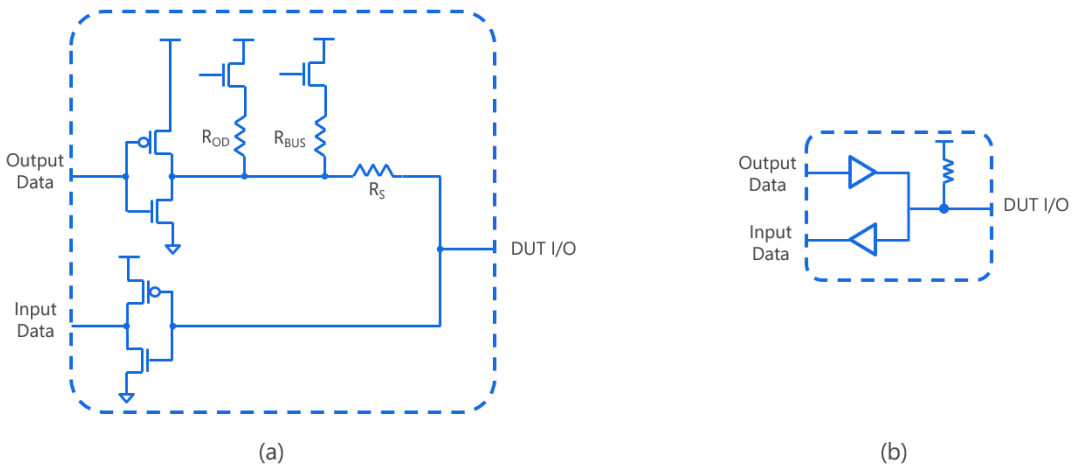


Figure 2: Functional representation of each I/O element. (a) Detailed view; (b) simplified representation.

The mapping between channels and ports is generally automatic within the SV6E-X. Simply select the protocol, and the Pinetree software will determine how channels are grouped into ports.

DEVICE CORES

The device core is the most important component in the SV6E-X because it is the firmware element that implements the native state machine of the licensed protocol being used. It provides true real-time pattern generation and branching based on device-under-test (DUT) responses. For example, when testing a MIPI I3C sensor device, the device core in the SV6E-X can act as a complete I3C Controller device, and it can be used to characterize the sensor to its pass/fail limits.

Please refer to the section Popular Protocols for further details on the device core functionality of your licensed protocol.

PROTOCOL ANALYZER CORES

A protocol analyzer core is a firmware component that samples data directly within each port (i.e. within each I/O element) and provides analysis based on the protocol being studied. For example, Figure 3 shows an I3C protocol analyzer trace. For this protocol, a port consists of two channels (SCL and SDA), and the protocol analyzer trace shows the behavior of both channels together as they transition through the different communications phases.

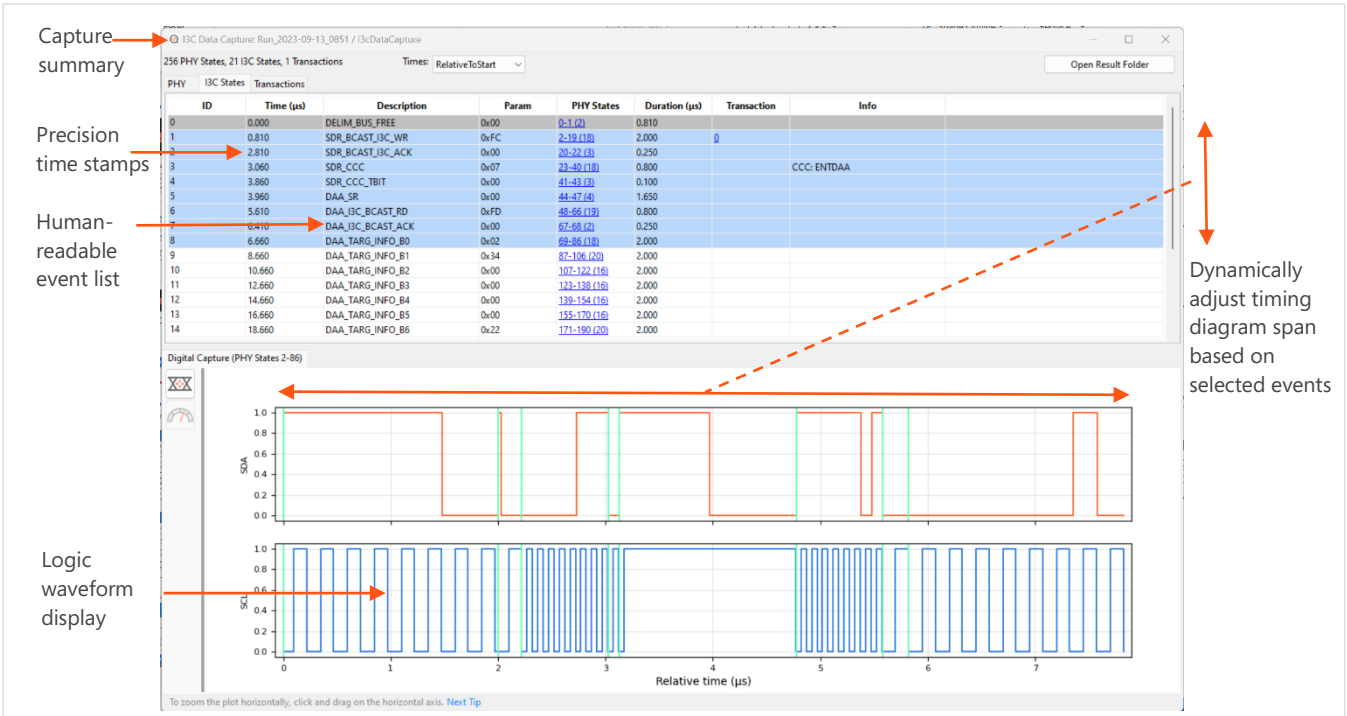


Figure 3: Example protocol analyzer trace (trace shown is for the MIPI I3C protocol).

REAL-TIME OSCILLOSCOPE CORE

Each SV6E-X contains an optional two-channel, 1 Gsps, 500 MHz real-time oscilloscope. The product also contains high fidelity analog switching circuitry that enables the attachment of the real-time oscilloscope channels to any channel on any I/O bank. For example, in I3C, the two channels of the real-time oscilloscope are connected to an SCL and SDA pair of any I3C port.

The real-time oscilloscope can be used as a stand-alone tool for measuring any signal type such as a power distribution network rail. More importantly, it can be used within the PurVue Analyzer™ framework. As part of PurVue Analyzer™, the real-time oscilloscope is time-synchronized with a protocol analyzer core to provide protocol-based oscilloscope triggering. This represents a significant productivity enhancement for CTS testing or for debug situations. An example of a stand-alone oscilloscope capture is shown in Figure 4 and an example of PurVue Analyzer™ capture is shown in Figure 5.

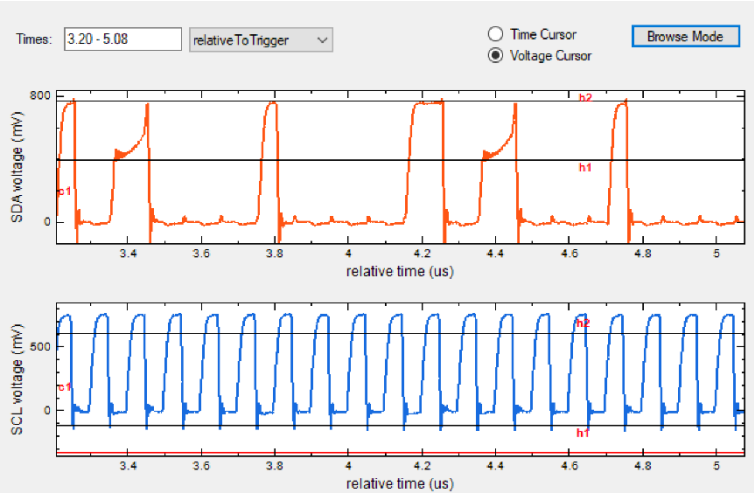


Figure 4: Standalone real-time oscilloscope waveforms.

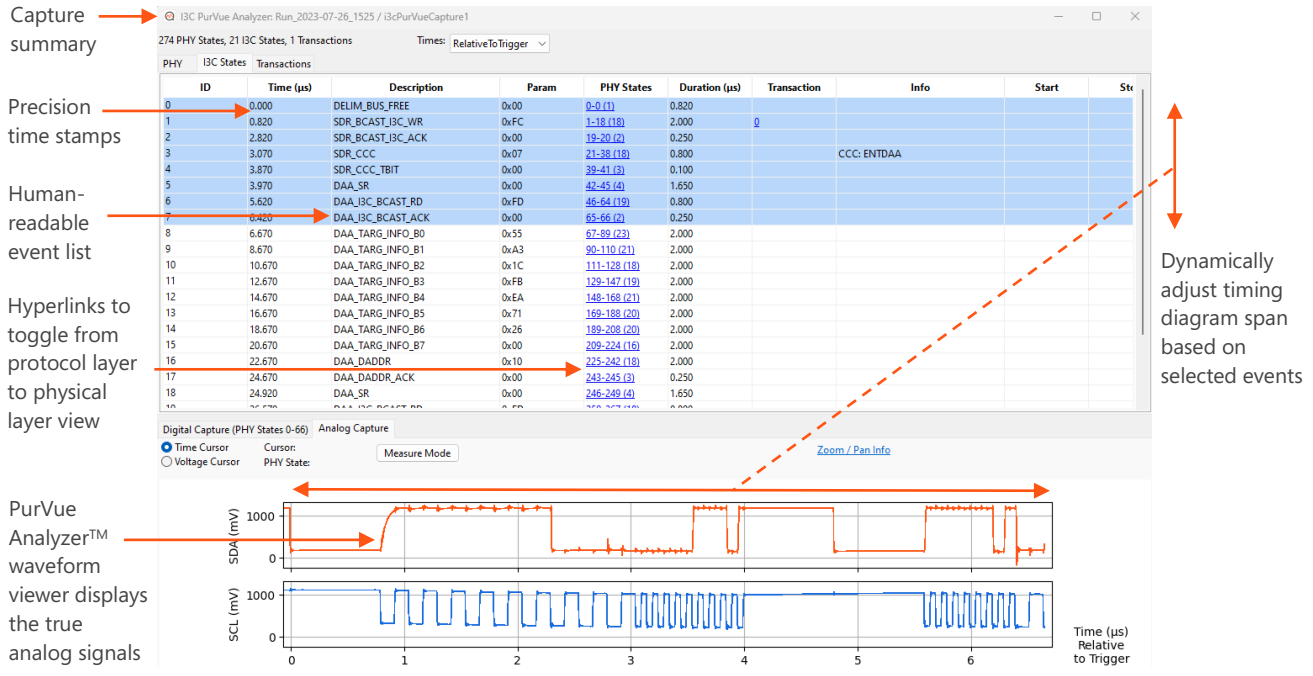


Figure 5: PurVue Analyzer™ trace for the MIPI I3C protocol.

PUTTING IT ALL TOGETHER: I3C EXAMPLE

Figure 6 shows how the different system components within the SV6E-X can be set up to create a realistic characterization solution for a MIPI I3C target device. Referring to the figure, a device core within the SV6E-X is configured as an I3C Controller class as shown (blue rectangle). Two channels are mapped to constitute an SCL/SDA port (white and green rectangle), an analyzer core is used to perform real-time data capture of the traffic going back and forth between the Controller device and the DUT (purple rectangle). Finally, the real-time oscilloscope core is attached to both pins in order to perform AC characterization.

Note how the analyzer core is connected behind the port whereas the real-time oscilloscope is connected in front of it. This is a true representation of the hardware architecture of the SV6E-X: logic captures are performed behind the I/O elements while oscilloscope captures are digitized directly on the connectors of the instrument. This yields the most accurate analog measurement.

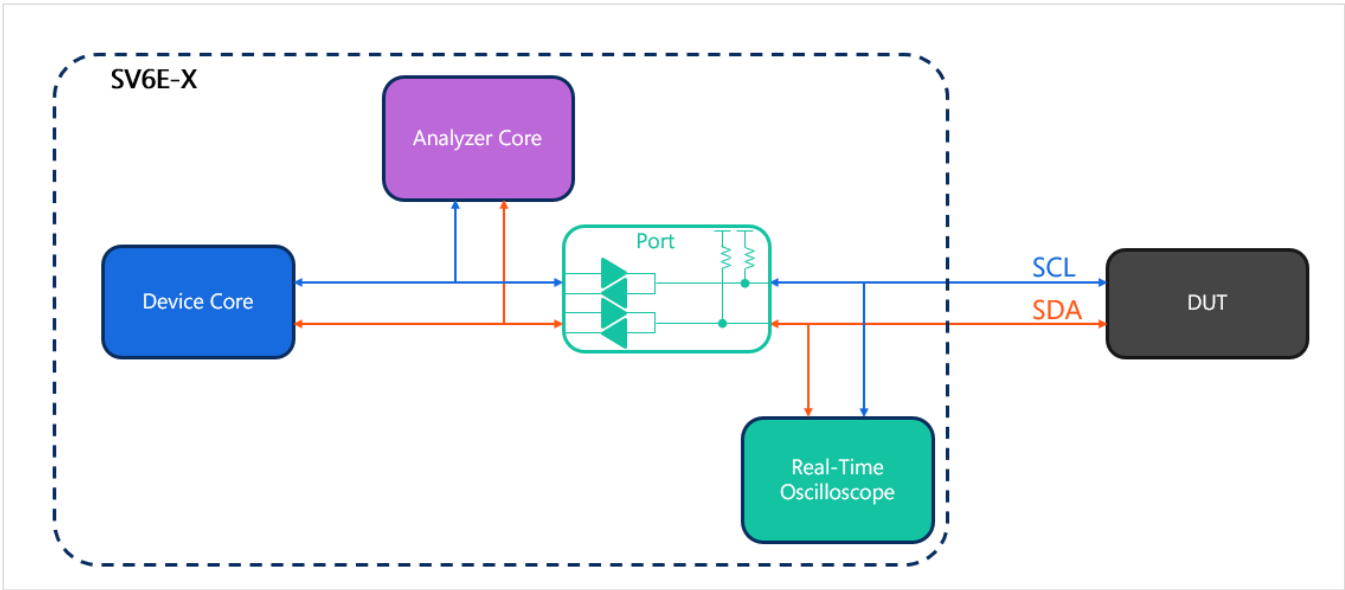


Figure 6: System components configured for testing an I3C target device.

Physical Connections

Figure 7 shows the physical connections on the SV6E-X module. The SV6E-X has two USB ports (USB 2.0 and USB 3.0) located on the left side of the chassis, which allows the SV6E-X to communicate directly with a PC. Power is provided to the SV6E-X module with a 12 V DC supply through a barrel connector. The recommended DC power supply, included with the SV6E-X module, is produced by CUI Incorporated, Part # CUI SDI65-12-U-P5.

Next, there are two GPIO and power banks, shown as GPIO & Power (Bank A) and GPIO & Power (Bank B). You can connect your device under test to either the DUT Interface (Bank A) or DUT Interface (Bank B), depending on your DUT's voltage range. See more information on the GPIO connections and signal pinouts in Tables 1 to 4 below. Finally, the SV6E-X has connections for a Reference Clock Output and a Reference Clock Input.

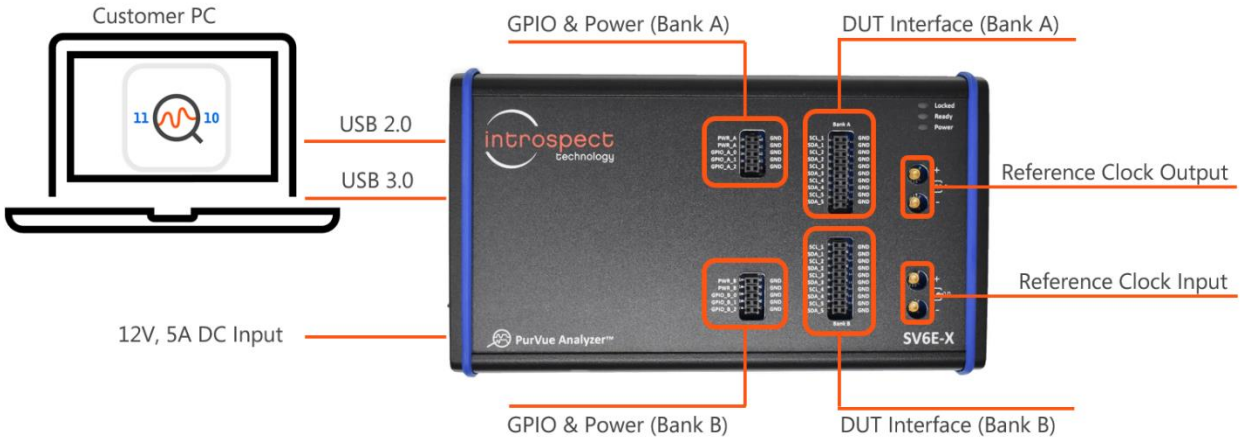


Figure 7: Physical connections of the SV6E-X module.

SIGNAL PINOUT INFORMATION

Table 1 shows the pinout for the DUT Interface on Bank A. The labels in this table refer to the pin definitions printed on the physical instrument, but it is important to note that the pin functionality depends on the licensed protocol. Please refer to the pinout definition of your selected protocol for the exact description of the pins.

TABLE 1: BANK A PINOUT

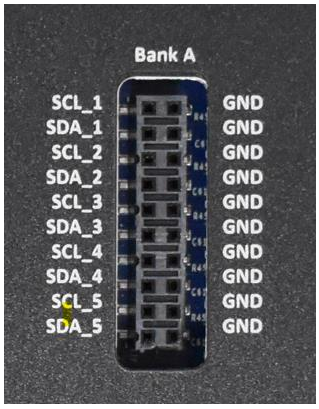
CONNECTOR DIAGRAM	PIN NUMBER	LABEL	SIGNAL DESCRIPTION
	2	SCL1	Fully capable I/O element that is attached to an internal device core, analyzer core, and/or real-time oscilloscope core
	4	SDA1	
	6	SCL2	
	8	SDA2	
	10	SCL3	
	12	SDA3	
	14	SCL4	
	16	SDA4	
	18	SCL5	
	20	SDA5	
	1, 3, 5, 7, 9, 11, 13, 15, 17, 19	Ground	Ground

Table 2 defines the GPIO connector pinout for Bank A. It is important to note that there are two power supplies available on this connector. One of them tracks the signals on this bank (PWR_A), but the other tracks the signals on Bank B (PWR_B). This second power supply is available here for convenience.

TABLE 2: BANK A GPIO PINS

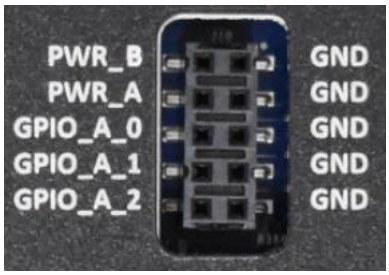
CONNECTOR DIAGRAM	PIN NUMBER	LABEL	SIGNAL DESCRIPTION
	2	PWR_B	Programmable DUT power supply. This supply tracks the logic "1" voltage level for all signals of Bank B (both the GPIO channels and the DUT interface channels).
	4	PWR_A	Programmable DUT power supply. This supply tracks the logic "1" voltage level for all signals of Bank A (both the GPIO channels and the DUT interface channels).
	6	GPIO_A_0	User configurable, input or output Logic "1" voltage = PWR_A voltage Logic "0" voltage = 0 V
	8	GPIO_A_1	User configurable, input or output Logic "1" voltage = PWR_A voltage Logic "0" voltage = 0 V
	10	GPIO_A_2	User configurable, input or output Logic "1" voltage = PWR_A voltage Logic "0" voltage = 0 V
	1, 3, 5, 7, 9	Ground	Ground

Table 3 shows the pinout for the DUT Interface on Bank B. The labels in this table refer to the pin definitions printed on the physical instrument, but it is important to note that the pin functionality depends on the licensed protocol. Please refer to the pinout definition of your selected protocol for the exact description of the pins.

TABLE 3: BANK B PINOUT

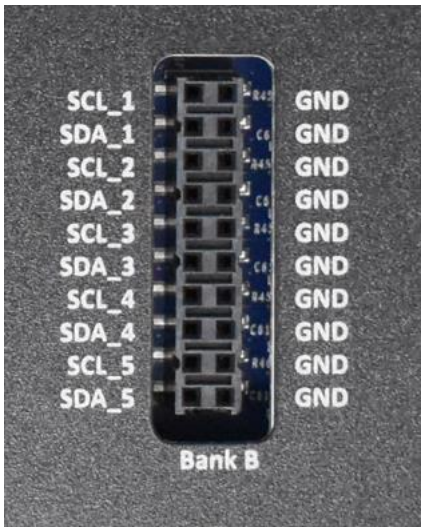
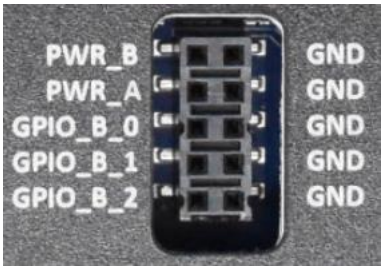
CONNECTOR DIAGRAM	PIN NUMBER	LABEL	SIGNAL DESCRIPTION
	2	SCL1	Fully capable I/O element that is attached to an internal device core, analyzer core, and/or real-time oscilloscope core
	4	SDA1	
	6	SCL2	
	8	SDA2	
	10	SCL3	
	12	SDA3	
	14	SCL4	
	16	SDA4	
	18	SCL5	
	20	SDA5	
	1, 3, 5, 7, 9, 11, 13, 15, 17, 19	Ground	Ground

Table 4 defines the GPIO connector pinout for Bank B. It is important to note that there are two power supplies available on this connector. One of them tracks the signals on this bank (PWR_B), but the other tracks the signals on Bank A (PWR_A). This second power supply is available here for convenience.

TABLE 4: BANK B GPIO PINS

CONNECTOR DIAGRAM	PIN NUMBER	LABEL	SIGNAL DESCRIPTION
	2	PWR_B	Programmable DUT power supply. This supply tracks the logic “1” voltage level for all signals of Bank B (both the GPIO channels and the DUT interface channels).
	4	PWR_A	Programmable DUT power supply. This supply tracks the logic “1” voltage level for all signals of Bank A (both the GPIO channels and the DUT interface channels).
	6	GPIO_B_0	User configurable, input or output Logic “1” voltage = PWR_B voltage Logic “0” voltage = 0 V
	8	GPIO_B_1	User configurable, input or output Logic “1” voltage = PWR_B voltage Logic “0” voltage = 0 V
	10	GPIO_B_2	User configurable, input or output Logic “1” voltage = PWR_B voltage Logic “0” voltage = 0 V
	1, 3, 5, 7, 9	Ground	Ground

Popular Protocols

This section describes protocols that are currently available for licensing on the SV6E-X. Note that the protocol roadmap keeps evolving, so if you require a protocol that is not listed here, please contact us directly at info@introspect.ca.

I3C, I3C BASIC, AND SIDEBANDBUS PROTOCOLS

PORT AND BANK DEFINITIONS

Bank A signal mapping is shown in Table 5 and Bank B signal mapping is shown in Table 6.

TABLE 5: I3C LOW-VOLTAGE PORT DEFINITIONS (BANK A)

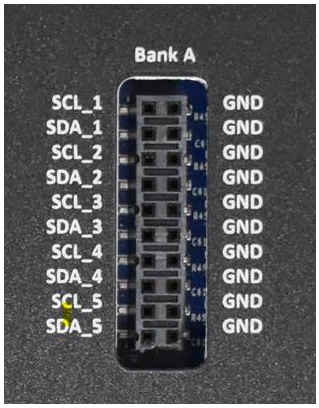
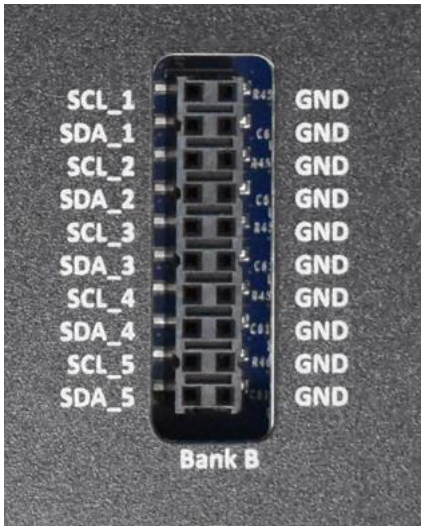
CONNECTOR DIAGRAM	PIN NUMBER	LABEL	SIGNAL DESCRIPTION
	2	SCL1	SCL1
	4	SDA1	SDA1
	6	SCL2	SCL2
	8	SDA2	SDA2
	10	SCL3	SCL3
	12	SDA3	SDA3
	14	SCL4	SCL4
	16	SDA4	SDA4
	18	SCL5	Not connected
	20	SDA5	Not connected
	1, 3, 5, 7, 9, 11, 13, 15, 17, 19,	Ground	Ground

TABLE 6: I3C HIGH-VOLTAGE PORT DEFINITIONS (BANK B)

CONNECTOR DIAGRAM	PIN NUMBER	LABEL	SIGNAL DESCRIPTION
	2	SCL1	SCL1
	4	SDA1	SDA1
	6	SCL2	SCL2
	8	SDA2	SDA2
	10	SCL3	SCL3
	12	SDA3	SDA3
	14	SCL4	SCL4
	16	SDA4	SDA4
	18	SCL5	Not connected
	20	SDA5	Not connected
	1, 3, 5, 7, 9, 11, 13, 15, 17, 19	Ground	Ground

For all I3C (and I2C) protocol implementations, each port consists of two I/O elements, one for SCL and one for SDA, as mentioned previously. Also, it is possible to use up to 4 ports simultaneously, but these ports all must be part of a single bank. That is, only one bank can be used at a time. Changing between banks happens in software and does not require any firmware update.

The difference between Bank A and Bank B is in the voltage range. Bank A is specified as a low-voltage bank, and it is capable of driving signals down to 0.8V. Bank B is specified as a high-voltage bank capable of driving up to 3.6V voltage levels. The detailed specifications of both banks are described later in this document.

DEVICE CORE CAPABILITIES

The I3C device core supports the MIPI I3C and MIPI I3C Basic specifications. It also supports derivative specifications such as JEDEC ones, and the complete list is included in Table 7.

Each SV6E-X device core can act as a controller and as a target, and it supports switching between controller and target roles through software commands. It also supports all interrupt capability and all error insertion requirements. Please refer to the Pinetree API for a detailed listing of all methods and all attributes of these device classes.

TABLE 7: I3C PROTOCOLS SUPPORTED BY SV6E-X DEVICE CORES

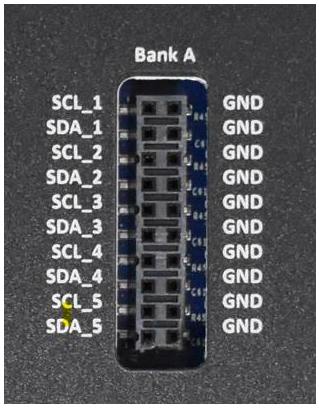
PROTOCOL FAMILY	DESCRIPTION AND CONDITIONS
MIPI I3C	MIPI I3C version 1.0 and 1.1 and 1.1.1 MIPI I3C Basic 1.0 and 1.1
JEDEC	JESD82-511 DDR5 RCD JESD403B Sideband Bus JESD300-5 SPD JESD301-1A PMIC JESD301-2 PMIC JESD302-1 TS5110 Thermal Sensor JESD302-1 TS5111 Thermal Sensor
I2C	Regular Fast Mode Fast Mode +
DMTF	Management Component Transport Protocol (MCTP) I3C Transport Binding Specification
SNIA	SFF-TA-1009

SPI, QUAD SPI, AND OCTAL SPI

PORT AND BANK DEFINITIONS

For the SPI license, only one port is available, and it is connected to Bank A of the SV6E-X. Table 8 shows the detailed pinout. As can be seen, the SV6E-X supports up to 8 data lanes in parallel, and these can all be clocked on a single clock domain defined by SCLK. It is understood that the lane configuration can be programmed dynamically in software. For example, the port can be changed into a Quad SPI bus in which there are only 4 data lanes (DATA1 to DATA4).

TABLE 8: SPI PINOUT (BANK A)

CONNECTOR DIAGRAM	PIN NUMBER	LABEL	SIGNAL DESCRIPTION
	2	SCL1	SCLK
	4	SDA1	CS
	6	SCL2	DATA1
	8	SDA2	DATA2
	10	SCL3	DATA3
	12	SDA3	DATA4
	14	SCL4	DATA5
	16	SDA4	DATA6
	18	SCL5	DATA7
	20	SDA5	DATA8
	1, 3, 5, 7, 9, 11, 13, 15, 17, 19	Ground	Ground

DEVICE CORE CAPABILITIES

The SPI core in the SV6E-X can act as a controller that can perform read and write transactions on any SPI target. It can do so in single data rate (SDR) mode as well as double data rate (DDR) mode. Additionally, the core contains a precision timing generator capable of adjusting data to clock setup time with a resolution of 100 ps.

The SPI device can also act as a target, and it contains built-in emulation modes for typical flash memories. Most importantly, even as a target, the SV6E-X SPI device core can adjust timing with a resolution of 200 ps, thus providing all-important capability for testing controller devices that send the SPI SCLK. That is, the SV6E-X can receive the SCLK and then injection fine-resolution delays on read-back data that is clocked by this SCLK. This is a challenging receiver test for SPI controllers, and it is available on the SV6E-X.

ANALYZER CAPABILITIES

The SPI analyzer core in the SV6E-X operates at an internal frequency of 200 MHz and samples data on the rising edge of the internal sampling clock. Thus, it can sample data with a resolution of 5 ns. Figure 8 shows a sample waveform for an 8-lane SPI bus. As can be seen, the data is distributed across eight

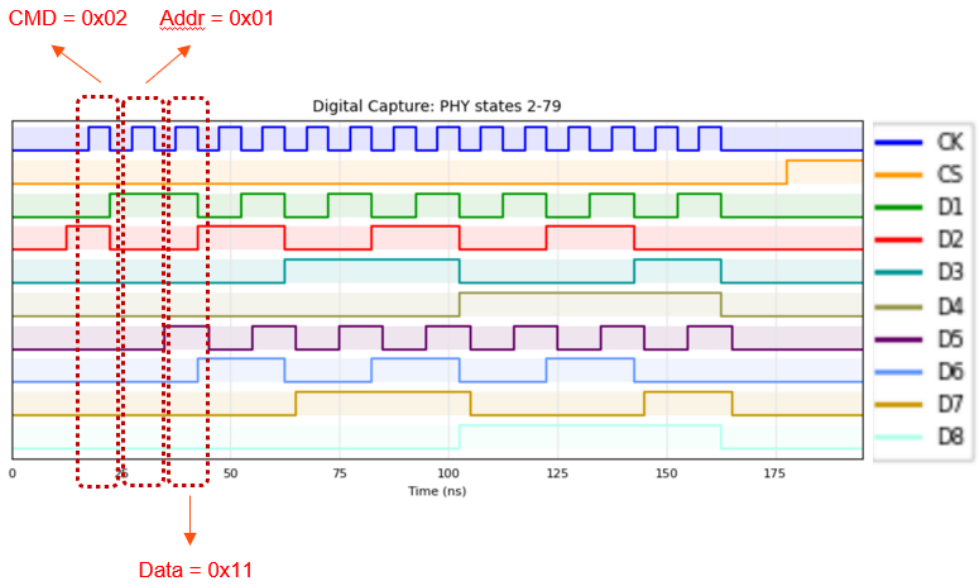


Figure 8: Protocol analyzer trace showing SPI testing across 8 parallel lanes.

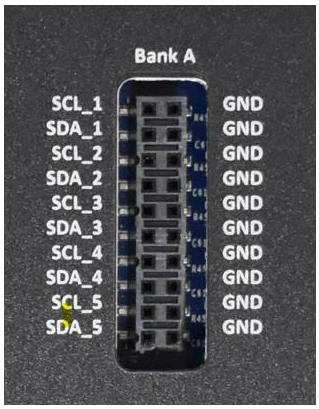
channels, thus transmitting an entire byte in only one clock cycle. Also shown in the trace is an example of how addressing is distributed across the data channels as well. Just like in the I3C protocol analyzer, the SPI analyzer can export its data to Python or to operating-system files for post-processing. Further details can be found within the Pinetree API documentation.

MIPI SOUNDWIRE

PORT AND BANK DEFINITIONS

Only Bank A is used for SoundWire testing, and its pin mapping is shown in Table 9. Like I3C, only 8 signal positions are used, thus exposing up to 4 SoundWire managers or peripherals.

TABLE 9: SOUNDWIRE PORT DEFINITIONS (BANK A)

CONNECTOR DIAGRAM	PIN NUMBER	LABEL	SIGNAL DESCRIPTION
	2	SCL1	SCL1
	4	SDA1	SDA1
	6	SCL2	SCL2
	8	SDA2	SDA2
	10	SCL3	SCL3
	12	SDA3	SDA3
	14	SCL4	SCL4
	16	SDA4	SDA4
	18	SCL5	Not connected
	20	SDA5	Not connected
	1, 3, 5, 7, 9, 11, 13, 15, 17, 19,	Ground	Ground

DEVICE CORE CAPABILITIES

Each device core can operate as a manager or as a peripheral. Additionally, the cores can run at frequencies up to 13 MHz in DDR mode. The following is a summary of the SoundWire features supported within the SV6E-X:

- Automatic device discovery and enumeration
- Frame synchronization
- Write, read, and ping command support
- Fine-resolution handover mechanisms
- Interrupt requests
- Parity checking

Ordering Information

Since the SV6E-X supports many protocols and many licenses, the order configurations can vary from application to application. The following table shows a summary of the key order codes (part numbers) for the most typical applications. As can be seen, a single SV6E-X instrument can be pre-configured at the factory with one protocol license such as I3C. Then, other licenses can be added at any time in the lifetime of the product. The PurVue Analyzer™ license can be added at any time as well.

TABLE 10: HARDWARE AND LICENSE ORDER CODES

PART NUMBER	NAME	KEY DIFFERENTIATORS
7206	SV6E-X - Mid-Frequency Digital Test Module -- I3C. Includes PC SW License (Perpetual)	Pre-configured with an I3C license
7207	PurVue Analyzer™ Integrated 1 Gsps Oscilloscope for SV6E-X	Option to provide PurVue Analyzer™ Protocol-Triggered Real-Time Oscilloscope to SV6E-X Mid-Frequency Digital Test Module. Can be added to any protocol license
7210	SV6E-X - Mid-Frequency Digital Test Module -- SoundWire. Includes PC SW License (Perpetual)	Pre-configured with a SoundWire license
7213	SV6E-X - Mid-Frequency Digital Test Module -- Octal SPI. Includes PC SW License (Perpetual)	Pre-configured with an SPI license
7209	SV6E-I3CL - I3C License for SV6E-X	I3C license
7212	SV6E-SoundWireL - SoundWire License for SV6E-X	SoundWire license
7215	SV6E-SPIL - Octal SPI License for SV6E-X	SPI license

Specifications

GENERAL SPECIFICATIONS

TABLE 11: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
I/O Elements			
Open-Drain Pull-Up Resistor	500	Ohms	Dynamically switchable
High-Keeper Pull-Up Resistor	10	kOhm	Dynamically switchable
Pin Capacitance	2.5	pF	
Bank A Voltages			
Minimum High Voltage	800	mV	
Maximum High Voltage	2020	mV	
High Voltage Resolution	1	mV	
Bank B Voltages			
Minimum High Voltage	1600	mV	
Maximum High Voltage	3600	mV	
High Voltage Resolution	1	mV	
Memory Capacity and Bandwidth			
On-board memory	1	GByte	DDR4 memory
Power Consumption			
DC Input Voltage	12	V	DC Input Voltage
Maximum Current Draw	2	A	Typical operating current draw
Reference Clocks			
Output Clock Minimum Frequency	10	MHz	Single-ended 1.8V LVCMOS
Output Clock Maximum Frequency	200	MHz	Single-ended 1.8V LVCMOS
Input Clock Minimum Frequency	10	MHz	Single-ended 1.8V LVCMOS
Input Clock Maximum Frequency	50	MHz	Single-ended 1.8V LVCMOS

PURVUE ANALYZER™ SPECIFICATIONS

TABLE 12: PURVUE ANALYZER™ SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
General Performance			
Number of Channels	2		
Channel Multiplexer Coverage	Bank A Bank B		Connected only to the DUT interface banks and not to the GPIO banks
Minimum Input Voltage	-300	mV	
Maximum Input Voltage	3600	mV	
Oscilloscope Resolution	12	bit	1 mV resolution at full input range
Oscilloscope Triggering			Oscilloscope captures are triggered by protocol events
Sampling Rate	1.0	Gsps	Maximum sampling rate
Analog Bandwidth	500	MHz	
Data Transfer (via USB 3.0)	5.0	Gbps	Provides rapid waveform uploads

I3C SPECIFICATIONS

TABLE 13: I3C FREQUENCY SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Operating Frequencies			
Minimum Open Drain Frequency	0.02	MHz	
Maximum Open Drain Frequency	5.0	MHz	
Minimum Push-Pull Frequency	0.02	MHz	
Maximum Push-Pull Frequency	13	MHz	
Minimum Legacy I2C Frequency	0.002	MHz	
Maximum Legacy I2C Frequency	1	MHz	

TABLE 14: I3C BUS TIMING SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
SCL / SDA Timing			
SDA Setup Time Range	1.0	UI	Specification for the timing from SCL falling edge to the following SDA edge, expressed as a fraction of the UI.
Independent SDA Setup Timing	Yes		SDA setup time is set independently for I3C Open Drain, I3C Push Pull, and I2C operation.
SCL to SDA Skew Injection Resolution	2.5*	ns	Timing resolution, SCL to SDA for 12.5 MHz Push-Pull Operation. Please see footnote below. A diagram of SDA setup time is shown in Figure 9 on the following page.
Duty Cycle Timing Resolution	10	ns	
Protocol Analyzer Timing Resolution	10	ns	PurVue Analyzer™ resolution is defined in Table 12.

*This 2.5 ns timing resolution may be selectively applied to any one of the parameters listed below. All other timing parameters may be set with 10 ns resolution.

Push-Pull SDA setup time
HDR / DDR Positive SDA setup time
HDR / DDR Negative SDA setup time
Start or Repeated Start hold time (t_{CAS} or t_{CASr})
Repeated Start setup time (t_{CBSr})
Stop setup time (t_{CBP})

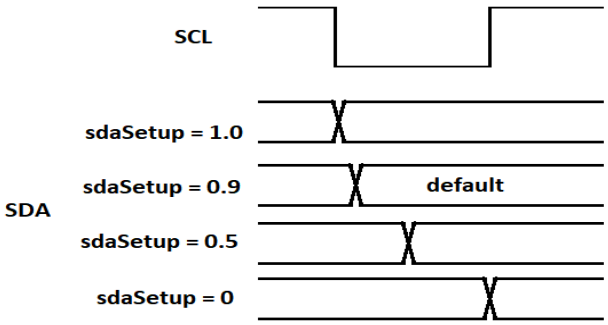


Figure 9: Definition of setup time for the I3C protocol.

TABLE 15: I3C MODES AND OPERATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Additional supported features			
Operations	CCC Direct RW Private RW Hot-Join IBI		
Signaling Modes	SDR HDR-DDR		
Mixed Bus Mode Support	Yes		
50 ns Spike Filter	Yes		Automatic for mixed bus mode
Error Injection	Yes		ACK/NACK behavior Flipped parity bit Setup time and hold time violations
Protocol Analysis	Yes		
Offline Capability / Tri-State Mode	Yes		Tri-state mode for SCL/SDA pins

SPI SPECIFICATIONS

TABLE 16: SPI SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Data Rate	200	MHz	Range: 10Mhz – 200MHz in steps of 1MHz
Data to SCLK Setup Time Range	+/- 2.0	UI	Applies to both SDR mode and DDR mode
Number of Delay Generators	2		Only two delay generators exist in the firmware, one for SCLK and one for all data lanes (DATA1 to DATA8). Thus, data setup and hold test time applies to all data channels at the same time
Controller-side setup time programming resolution	100	ps	This is the resolution when the SV6E-X is acting as an SPI Controller and generating the SCLK to drive the DUT
Target-side setup time programming resolution	200	ps	This is the resolution when the SV6E-X is acting as an SPI Target and receiving the SCLK from the DUT

SOUNDWIRE SPECIFICATIONS

TABLE 17: SOUNDWIRE SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Physical Layer			
Bus Hold Resistor	7	kOhm	Holds the last driven state on the I/O element
Data Encoding	Modified NRZI		Follows the SoundWire v1.2.1 specifications
Operating Frequencies			
Minimum Frequency	0.02	MHz	
Maximum Frequency	13	MHz	
Timing Parameters			
Data Setup Time Range	1.0	UI	
Independent Setup Timing	Yes		All operating modes of SoundWire are supported
Clock to Data Skew Injection Resolution	2.5	ns	
Duty Cycle Timing Resolution	10	ns	
Protocol Analyzer Timing Resolution	10	ns	PurVue Analyzer™ resolution is defined in Table 12

REVISION NUMBER	HISTORY	DATE
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