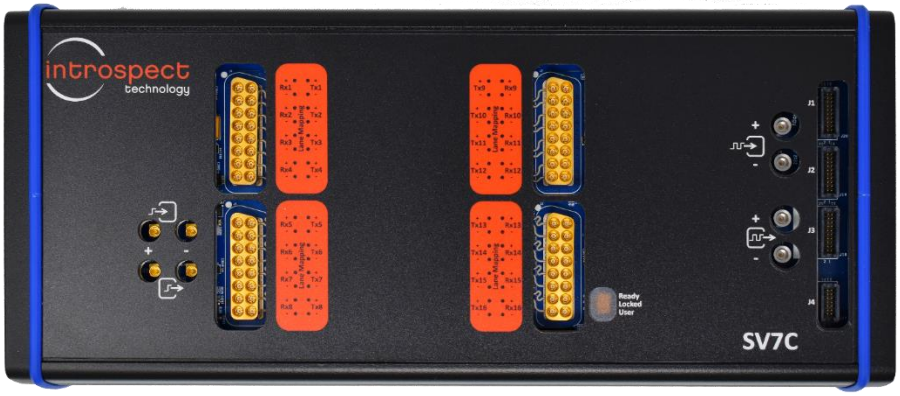
QUICK START GUIDE

SV7M-DDRPA

LPDDR5 Protocol Analyzer

M SERIES



Published in Canada on June 3, 2024
EN-G069E-E-24155

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Table of Contents

Introduction

OVERVIEW

The SV7M-DDRPA LPDDR5 Protocol Analyzer is a solution for validating and debugging LPDDR5 memory interfaces. Providing support for 1 channel of a LPDDR5 DRAM, this analyzer can capture read and write commands, and it is able to provide deep analysis of all protocol events on the LPDDR5 bus. Coupled with a Remote Sampling Head (RSH) solution, the SV7M-DDRPA is ideal for measuring new LPDDR5 components running at 8533 Mbps.

QUICK START DOCUMENTATION

This Quick Start Guide will provide the information required for a user to set up the SV7M-DDRPA LPDDR5 Protocol Analyzer by providing detailed descriptions and diagrams for all the required connections. A brief introduction to using the protocol analyzer will also be given.

HARDWARE REQUIREMENTS

- (QTY = 2) SV7C-17 Personalized SerDes Testers (Introspect # 5917)
- (QTY = 2) 12V / 25A Power Supply Units (TDK-Lambda DTM300PW120D1)
- (QTY = 2) USB 3.0 to mini-USB cables for connection between each SV7C and a PC
- (QTY = 2) USB-C to USB-C cables for high-speed connection between each SV7C and a PC
- (QTY = 1) SV7C Differential Remote Sampling Head (Introspect # 7157)
- (QTY = 3) SV7C Single-Ended Remote Sampling Head (Introspect # 7158)
- (QTY = 4) 12V / 5A Power Supply Units (CUI Inc SDI65-12-UD)
- (QTY = 2) Huber+Suhner MXP[16:1] to 2 MXP[16:9] cables (Introspect # 4803)
- (QTY = 2) Huber+Suhner MXP[16:1] to 2 MXP[8:1] cables (Introspect # 4804)
- (QTY = 2) 12-inch MMPX to MMPX cables (Huber+Suhner MF86/11MMPX/11MMPX/305mm)
- (QTY = 2) Phase-matched SMP to SMP cables (Introspect # 4806)
- (QTY = 2) SMA male to SMA male adapters (example part # Amphenol RF 132168)
- (QTY = 1) 8-wire 14-pin to 14-pin GPIO cable for the SV7C-to-SV7C connection (GPIO Cable A)
- (QTY = 2) 13-wire 20-pin to 14-pin GPIO cable for the SV7C-to-RSH connection (GPIO Cable B)
- (QTY = 2) 14-wire 14-pin to 14-pin GPIO cable for the RSH-to-RSH connection (GPIO Cable C)
- (QTY = 1) PC for running Introspect's software environment, Pinetree

FOR USE WITH THE INTERPOSER

- (QTY = 1) Differential IPEX Adapter (Introspect # 4868)
- (QTY = 3) Single-Ended IPEX Adapter (Introspect # 4869)
- (QTY = 1) LPDDR5 DRAM Interposer (Introspect # 4867)

FOR USE WITHOUT THE INTERPOSER

- (QTY = 1) Differential Termination Board (Introspect # 7162)
- (QTY = 3) Single-Ended Termination Board (Introspect # 7161)
- (QTY = 35) SMA female to SMPM female adapters (example part # Johnson 134-1001-003)

IMPORTANT NOTE

For fully phase aligned operation across all 32 TX channels, a calibration must be performed on the two SV7C modules. This calibration may be performed in the factory before shipment of a pair of units, or it may be performed "in-field".

Step by Step Guide

MULTI-BOX FORM FACTOR CONNECTION

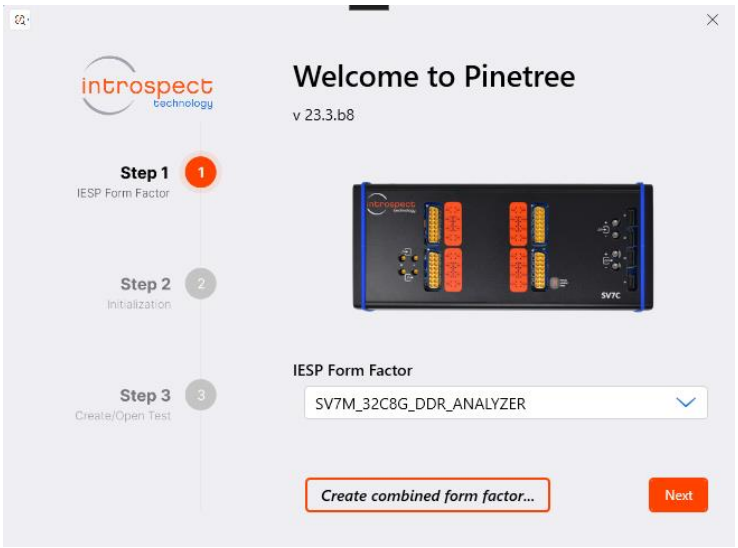

Figure 1: Opening Pinetree with the SV7M_32C8G_DDR_ANALYZER form factor.

1. Open Pinetree with the SV7M_32C8G_DDR_ANALYZER form factor as in Figure 1 above and create a new test.
2. Connect the USB cables from your PC to both SV7C boxes and turn the boxes on. Open the "ConnectionConfig" tool (IESP -> ConnectionConfig). Set the serial numbers for box 1 and box 2 accordingly as in Figure 2 below. The serial number can be found underneath the SV7C box. It is important to externally label the first SV5C unit as "Box 1" and the second unit as "Box 2". This labelling must be kept consistent during subsequent usage.

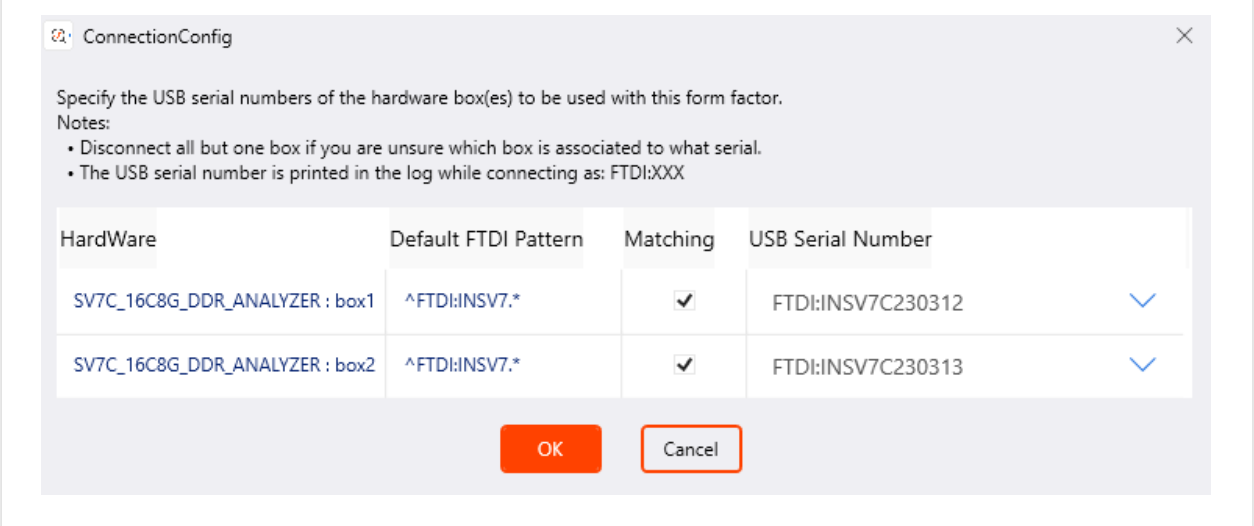

Figure 2: ConnectionConfig tool.

3. Close the "ConnectionConfig" tool as well as the Pinetree instance. Re-open a new test as in Step 1. Connect to both SV7C boxes (IESP -> Connect). You should see a successful connection to both boxes as in Figure 3 below.

```
Connecting to serialNum 'FTDI:INSV7C230312A'
Connected to subPart 'SV7C_16C17G_box1_A'
Connecting to serialNum 'FTDI:INSV7C230312B'
Connecting to serialNum 'FTDI:INSV7C230313A'
Connected to subPart 'SV7C_16C17G_box2_A'
Connecting to serialNum 'FTDI:INSV7C230313B'
Initializing IESP hardware/firmware
formFactor: SV7C_32C8G_DDR_ANALYZER
firmware for SV7C_32C8G_DDR_ANALYZER: FWIESPSV7C02B001,FWIESPSV7C02B001
Doing post-connection initialization
```

Figure 3: Successful connection.

SV7C CONNECTION DIAGRAMS

The required connections of the two SV7C modules are given in Figure 4 below.

The MMPX cables must be connected to the output on Box 1 and the input on Box 2 as indicated in red in Figure 4. The SMP cables must be connected to the output on Box 1 and the input on Box 2 as indicated in blue in Figure 4. The positive connector of Box 1 must go to the positive connector on Box 2 for both the MMPX and SMP cables.

If the MMPX cables or SMP cables have an SMA output, ensure that they are combined with SMA adapters to create MMPX to MMPX and SMP to SMP cables.

The 8-wire 14-pin to 14-pin GPIO cable, labeled 'A: SV7C to SV7C', must be used to connect the 2 SV7Cs as indicated in green in Figure 4. The side that is labeled 'Box 1' should go in the 'J4' slot of Box 1, and the side that is labeled 'Box 2' should go in the 'J4' slot of Box 2.

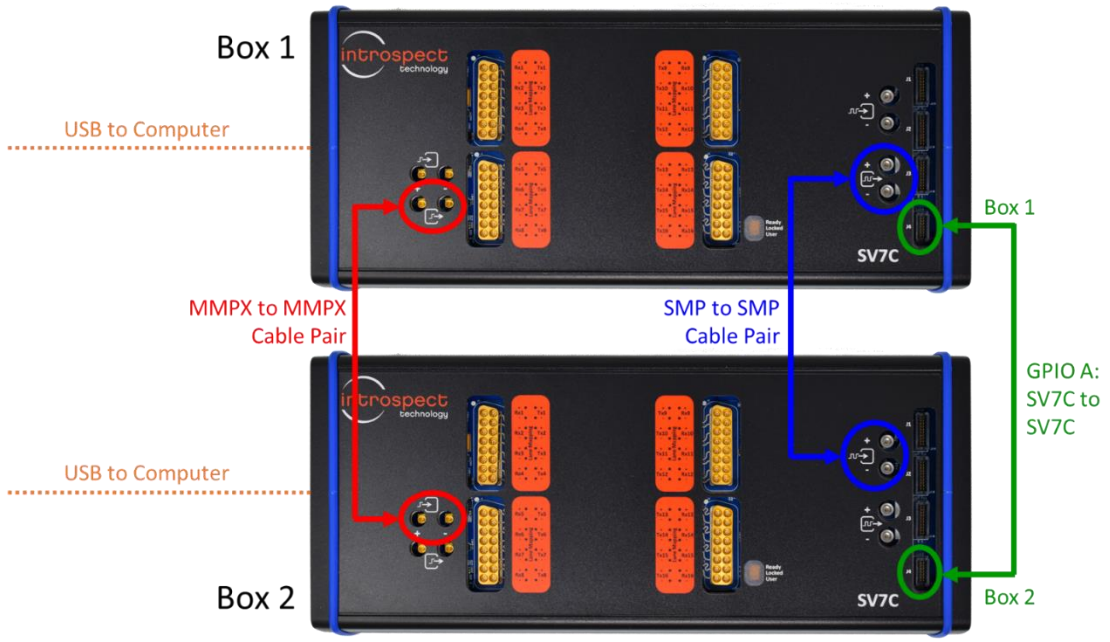

Figure 4: Block diagram of required connections between SV7C modules.

These connections will allow these two 16-channel units to operate as a single 32-channel system. The channels on Box 1 will be referred to as channels 1 to 16. The channels on Box 2 will be referred to as

channels 17 to 32. The connections defined in the above diagram will be referred to as the "32 Channel Connections".

RSH CONNECTION DIAGRAM

The required connections of the two SV7C modules to the 4 RSHs are given below. Figure 5 shows the setup required when using the interposer. Figure 6 shows the setup required when using the termination board adapters. The 32 channel connections made in the previous section must be kept for both setups.

SETUP REQUIRED WITH THE USE OF THE INTERPOSER OR WITH THE USE OF THE TERMINATION BOARD ADAPTERS

There are 4 RSH units being used. The first is a differential RSH, and the three others are single-ended RSHs. SV7C Box 1 will be connected to RSH 1 and 2. SV7C Box 2 will be connected to RSH 3 and 4.

The 13-wire 20-pin to 14-pin GPIO cables, labeled 'B: SV7C to RSH', must be used to connect the SV7C Box 1 to RSH 1 and SV7C Box 2 to RSH 3. The connection is indicated in green in Figure 5 and Figure 6. The 20-pin side, labeled 'SV7C', should go in the 'J3' slot of the SV7C, and the 14-pin side, labeled 'RSH', should go in the 'Control In' slot of RSH 1 or 3.

The 14-wire 14-pin to 14-pin GPIO cables, labeled 'C: RSH to RSH', must be used to connect the RSH 1 to RSH 2 and RSH 3 to RSH 4. The connection is indicated in blue in Figure 5 and Figure 6. This cable does not have a specified input or output side. One side should go in the 'Control Out' slot of RSH 1 or 3, and the other side should go in the 'Control In' side of RSH 2 or 4.

Cable types 4803 and 4804 will be used to send the captured signal from the RSH to the SV7C. Cable 4803 has an MXP end with pins 1 to 16 populated splitting to two MXP ends with pins 9 to 16 populated in each. Cable 4804 has an MXP end with pins 1 to 16 populated splitting to two MXP ends with pins 1 to 8 populated in each.

- RSH 1 should have the fully populated side of cable 4803 connected to it. Pins 1 to 8 should be going to RX[12:9] on SV7C Box 1. Pins 9 to 16 should be going to RX[16:13] on SV7C Box 1.
- RSH 2 should have the fully populated side of cable 4804 connected to it. Pins 1 to 8 should be going to RX[4:1] on SV7C Box 1. Pins 9 to 16 should be going to RX[8:5] on SV7C Box 1.
- RSH 3 should have the fully populated side of cable 4803 connected to it. Pins 1 to 8 should be going to RX[12:9] on SV7C Box 2. Pins 9 to 16 should be going to RX[16:13] on SV7C Box 2.
- RSH 4 should have the fully populated side of cable 4804 connected to it. Pins 1 to 8 should be going to RX[4:1] on SV7C Box 2. Pins 9 to 16 should be going to RX[8:5] on SV7C Box 2.

SETUP REQUIRED WITH THE USE OF THE INTERPOSER

The interposer will serve to provide convenient and non-intrusive attachment points for the active probes. The IPEX cables connected to the RSHs will be connected to the interposer as seen in Figure 5. The differential 20-pin IPEX cable must be connected to the differential RSH. The single-ended 10-pin IPEX cables must be connected to the single-ended RSHs.

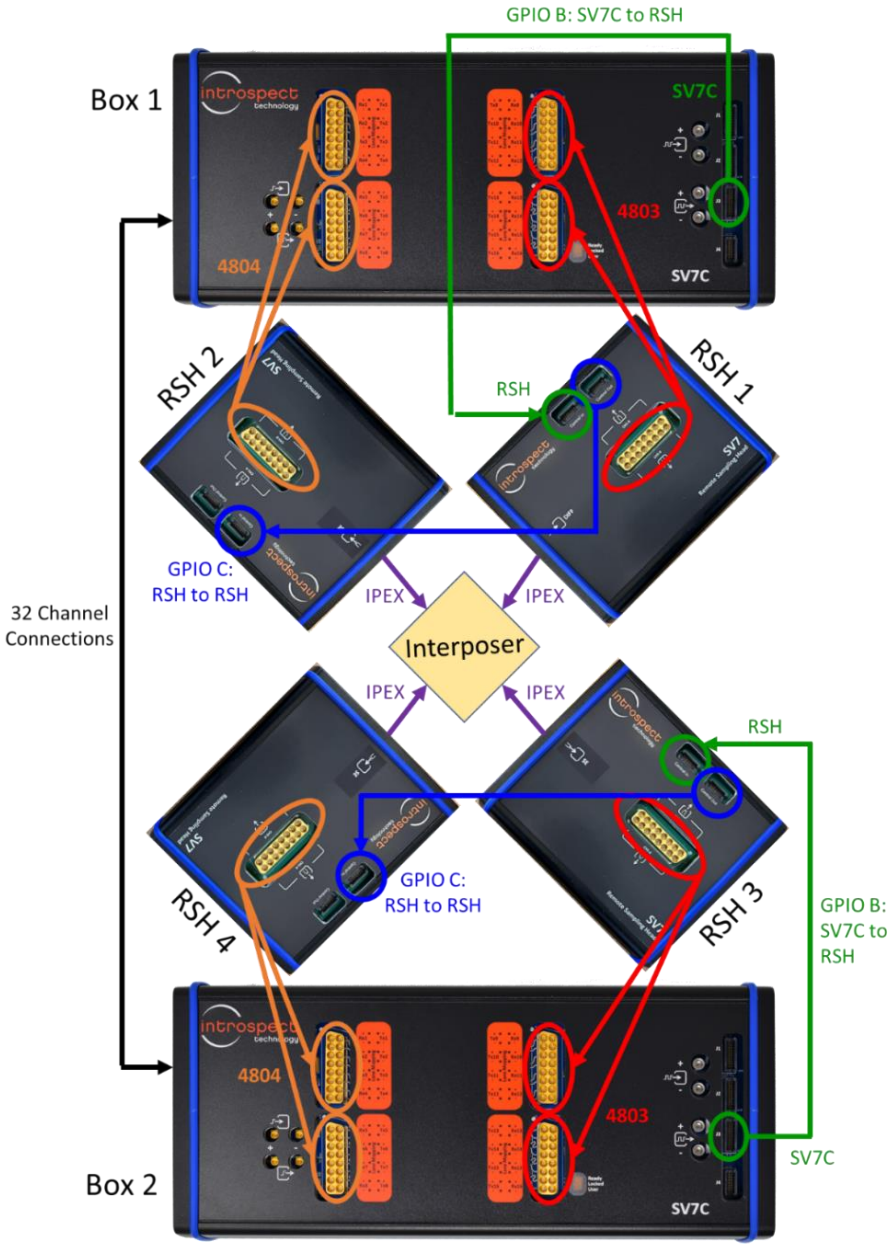

Figure 5: Block diagram of required connections between the SV7Cs and the RSHs with the use of the interposer.

SETUP REQUIRED WITH THE USE OF THE TERMINATION BOARD ADAPTERS

The termination board adapters will provide SMA endings for all the signals to be connected to the setup without the need for a pre-set mapping. The signals will drive into the termination board adapters who are attached to the RSHs as seen in Figure 6. The differential 13-pin termination board adapter must be connected to the differential RSH. The single-ended 8-pin termination board adapters must be connected to the single-ended RSHs.

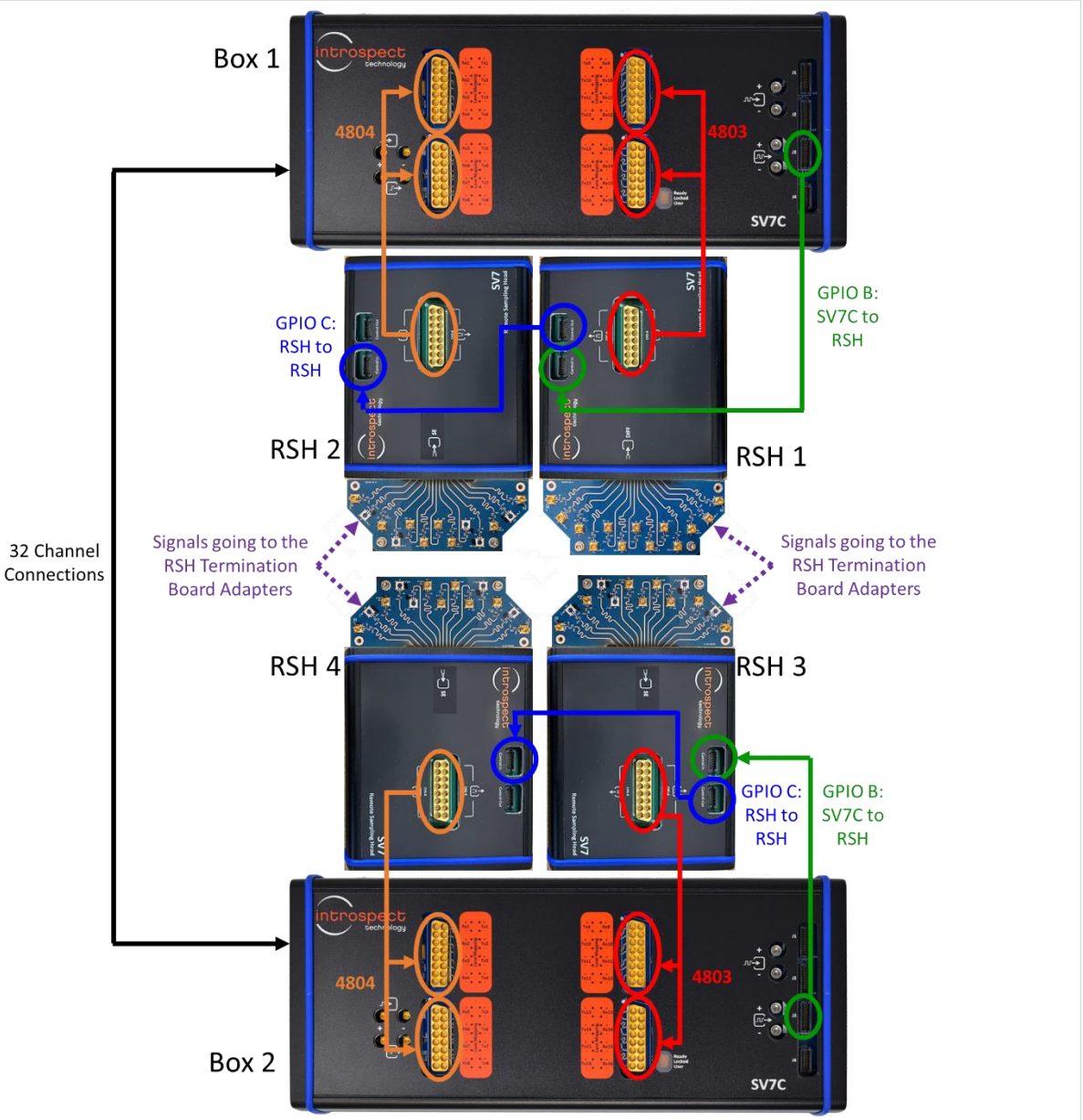

Figure 6: Block diagram of required connections between the SV7Cs and the RSHs with the use of the term boards.

LPDDR5 SIGNAL CONNECTIONS

TABLE 1: SV7M LPDDR5 PA SIGNAL CONNECTIONS

SV7C CHANNEL	RSH CHANNEL	LPDDR5 CHANNEL
Box 1 RX 1	RSH 2 Pin 1	CA1_A
Box 1 RX 2	RSH 2 Pin 2	CA2_A
Box 1 RX 3	RSH 2 Pin 3	CA3_A
Box 1 RX 4	RSH 2 Pin 4	CA5_A
Box 1 RX 5	RSH 2 Pin 5	DMI0_A
Box 1 RX 6	RSH 2 Pin 6	CA4_A
Box 1 RX 7	RSH 2 Pin 7	CA6_A
Box 1 RX 8	RSH 2 Pin 8	DMI1_A
Box 1 RX 9	RSH 1 Pin 1_P/N	RDQS0t/c_A
Box 1 RX 10	RSH 1 Pin 2_P/N	WCK0t/c_A
Box 1 RX 11	RSH 1 Pin 3	CA0_A
Box 1 RX 12	RSH 1 Pin 4	CS1_A
Box 1 RX 13	RSH 1 Pin 5_P/N	WCK1t/c_A
Box 1 RX 14	RSH 1 Pin 6_P/N	CKt/c
Box 1 RX 15	RSH 1 Pin 7_P/N	RDQS0t/c_A
Box 1 RX 16	RSH 1 Pin 8	CS0_A
Box 2 RX 1	RSH 4 Pin 1	DQ13_A
Box 2 RX 2	RSH 4 Pin 2	DQ14_A
Box 2 RX 3	RSH 4 Pin 3	DQ11_A
Box 2 RX 4	RSH 4 Pin 4	DQ9_A
Box 2 RX 5	RSH 4 Pin 5	DQ12_A
Box 2 RX 6	RSH 4 Pin 6	DQ15_A
Box 2 RX 7	RSH 4 Pin 7	DQ10_A
Box 2 RX 8	RSH 4 Pin 8	DQ8_A
Box 2 RX 9	RSH 3 Pin 1	DQ5_A
Box 2 RX 10	RSH 3 Pin 2	DQ6_A
Box 2 RX 11	RSH 3 Pin 3	DQ7_A
Box 2 RX 12	RSH 3 Pin 4	DQ4_A
Box 2 RX 13	RSH 3 Pin 5	DQ3_A
Box 2 RX 14	RSH 3 Pin 6	DQ1_A
Box 2 RX 15	RSH 3 Pin 7	DQ2_A
Box 2 RX 16	RSH 3 Pin 8	DQ0_A

REVISION NUMBER	HISTORY	DATE
1.0	Document Release	July 24, 2023
1.1	Added LPDDR Interposer Item number	August 16, 2023
1.2	Updated Table 1 to reflect the new revision of the Interposer; updated hardware requirements	June 3, 2024

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