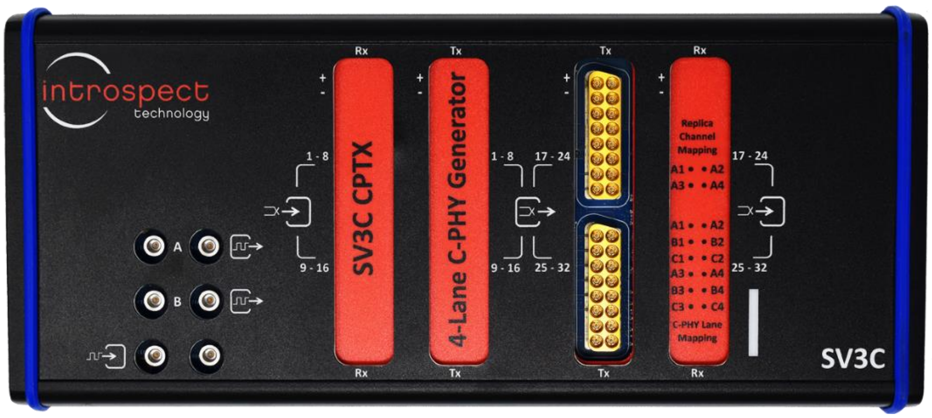
Ordering Information:

DATA SHEET

SV3C-CPTX

MIPI C-PHY Generator

C SERIES



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Introduction

OVERVIEW

The SV3C-CPTX C-PHY Generator is an ultra-portable, high-performance instrument that enables exercising and validating MIPI C-PHY receiver ports. Capable of generating any traffic and being completely data-rate agile, the C-PHY generator includes analog parameter controls that enable gaining deep insights into receiver sensitivity performance and skew/jitter tolerance.

The C-PHY Generator operates using the highly versatile Pinetree software environment. This environment allows for automating receiver tests such as voltage sensitivity or wire-skew tolerance. The environment also includes MIPI pattern compiler tools that enable the generation of complete DSI or CSI packets such as those characteristics of colour bars or active image frames.

This document describes the electrical characteristics and key specifications of the C-PHY Generator. Please refer to Pinetree documentation for additional operating instructions.

KEY FEATURES

- Parallel physical layer validation
- Interface test
- Plug-and-play system-level validation

KEY BENEFITS

- Any-rate operation and global timing parameter control
- Per-wire skew injection with < 1 ps resolution
- Per-wire voltage level control
- Per-wire LP generation
- State of the art programming environment based on the highly intuitive Python language
- Reconfigurable, protocol customization (on request)

ORDERING INFORMATION

This product is part of the SV3C family of MIPI generator products. The following table describes the part numbers and key feature differentiators.

TABLE 1: ORDERING PART NUMBERS FOR THIS PRODUCT

PART NUMBER	NAME	KEY DIFFERENTIATORS
4586	SV3C-CPTX	C-PHY only (this data sheet)
4593	SV3C Tx PHY Upgrade	License to add the D-PHY functionality

Feature Description

OVERALL BLOCK DIAGRAM AND SIGNAL GENERATION CONCEPTS

The SV3C-CPTX is a pattern generator capable of creating both LP and HS data streams across four C-PHY lanes simultaneously. Illustrated in Figure 1, the pattern generator architecture offers individual control over LP events, HS events, and global timing events on a per-wire basis. Thus, it provides complete electrical test coverage in a manner similar to AWG solutions while still being versatile enough to generate compliant CSI-2 packets and video frames from within a seamless software environment.

Built into the HS generators within the SV3C-CPTX are dedicated hardware C-PHY mapper and encoder circuits as shown in Figure 1. This allows for tremendous ease of use as will be described in later sections of this document. Specifically, when defining packet transmissions, the user need not construct wire states or transitions manually (unless he/she so desires) and can just define 16-bit integer payload data.

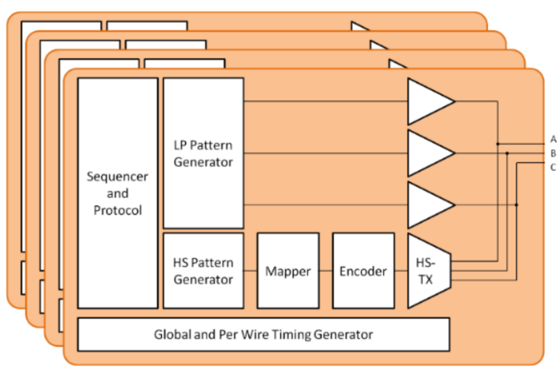


Figure 1: High-level block diagram of SV3C-CPTX 4-Lane C-PHY Generator.

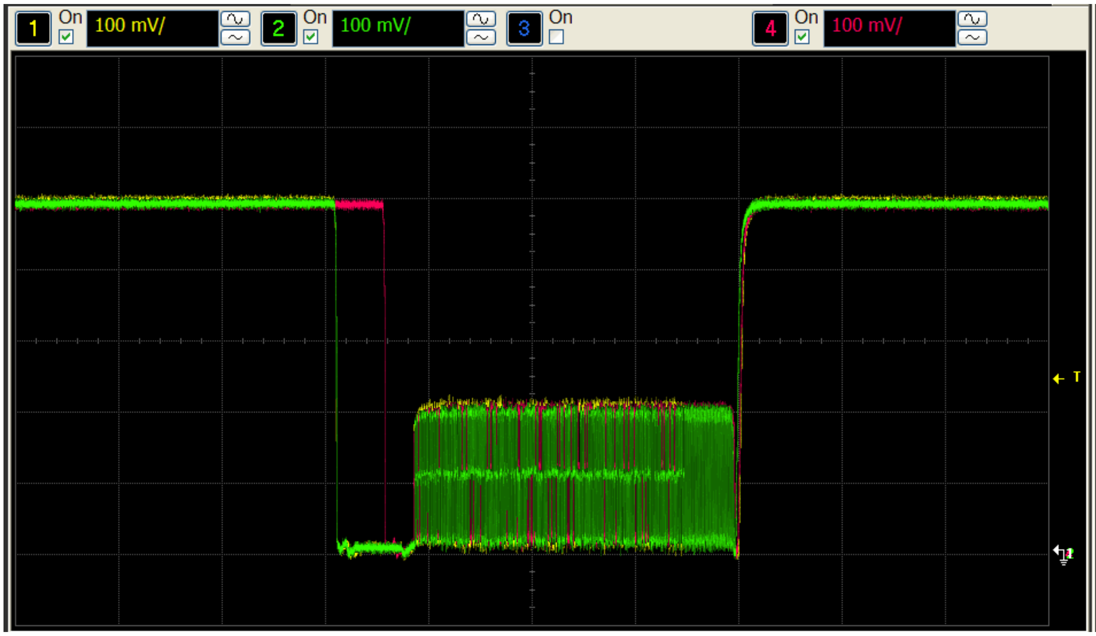


Figure 2: Global waveform showing LP and HS C-PHY transmissions on one lane (3 wires).

Figure 2 shows a packet transmission using the C-PHY generator. As can be seen, the packet starts from the STOP state, enters HS mode, and then transmits three-phase encoded data on the three wires. In the next section, we will describe how one can define such packet transmissions both from a payload perspective and a timing/voltage stress perspective.

BURST-MODE PATTERN DEFINITION AND GENERATION

In its most typical use case, the SV3C-CPTX generator is programmed to generate payload data as shown in Figure 3. The payload data is highlighted in the figure, and it can consist of fixed Test Patterns (e.g. PRBS data) or active packets as part of a video frame.

When it comes to Test Pattern transmission, Figure 4 illustrates how packet length is not necessarily constrained to be equal to Test Pattern size in the SV3C-CPTX generator. In fact, packet size can be much larger than Test Pattern length. For example, the Test Pattern can be a very short 16-bit or 32-bit sequence, and the packet size can be much larger. In this case, the Test Pattern is assumed to repeat continuously within a packet as shown in Figure 4.

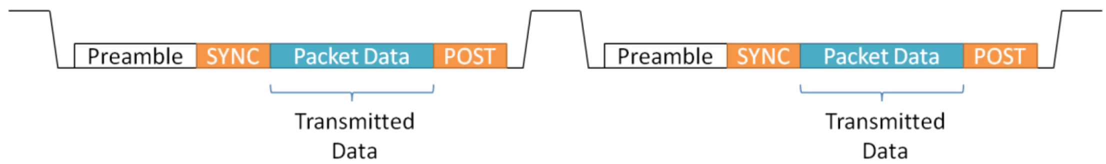


Figure 3: Basic concept of packet transmission.

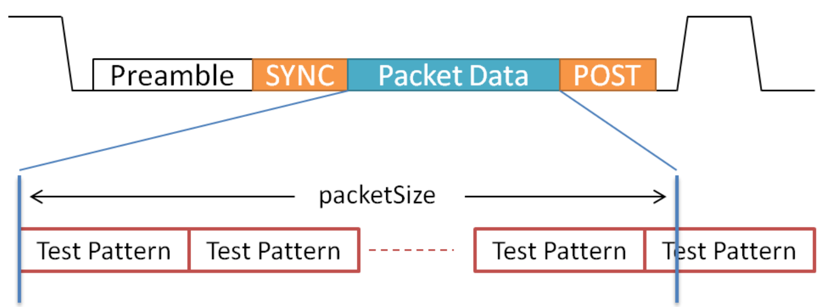


Figure 4: Distinction between Test Pattern length and packet size when transmitting fixed patterns in burst mode.

Defining the HS pattern to be transmitted is performed using the cphyPattern component within the Pinetree software as shown in Figure 5. Using this component, one is able to define the payload data within a transmission using high-level software commands. For example, shown in the figure is an array of 8 different 16-bit integer values representing counts from 1 to 8 and defined in the 'hsData' parameter of the cphyPattern component. When declared in this manner, the packet transmission in Figure 3 would play the 8 integer values within the active portion of the packet after automatic three-phase mapping and encoding in hardware.

In order to generate PRBS payload data within a packet, the 'hsDataMode' parameter of the cphyPattern component can be set to PRBS and the appropriate polynomial order and seed values can be selected.

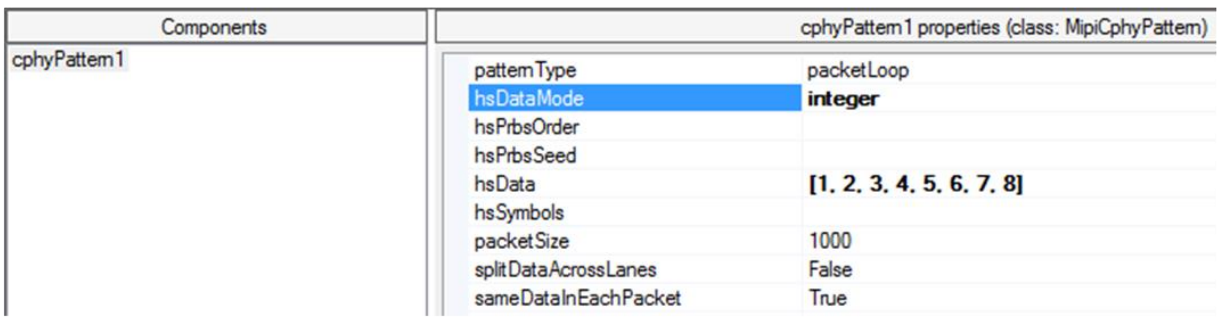


Figure 5: Data definition method within the Pinetree software.

GLOBAL TIMING PARAMETER CONTROLS

Similar to payload data definition, the SV3C-CPTX allows for controlling global timing parameters, and this is useful for automatically verifying HS receiver functionality under varying timing conditions. Figure 6 shows the cphyPattern component again with additional parameters related to packet timings. As can be seen, parameters such as preBeginNumUI and postNumUI allow for varying the timings associated with starting HS transmissions and ending them. Similarly, parameters such as lp000Duration allow for varying the preparation (termination enable) period when testing receivers in burst mode.

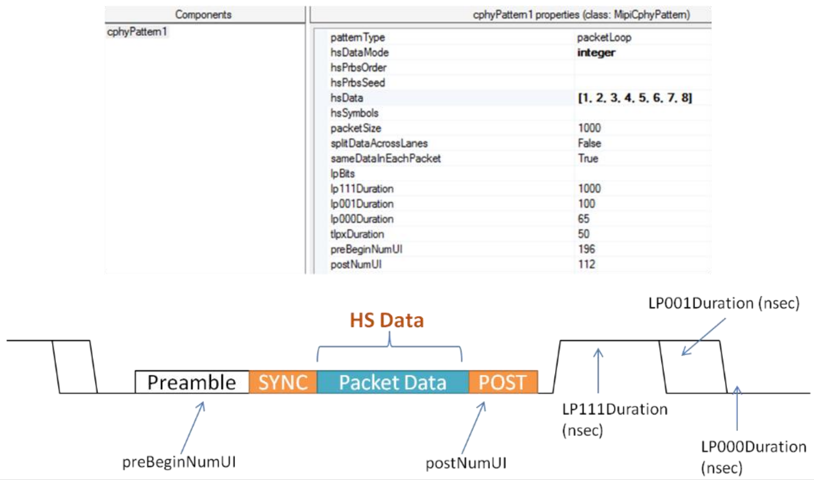


Figure 6: Global timing parameter control from within the cphyPattern component.

It is interesting at this stage to highlight another pattern generation feature of the SV3C-CPTX. It was mentioned in the previous section that payload data can be entered in integer format. However, if there is a need to define data in symbol format, or – better yet – to quickly verify what an integer value corresponds to in C-PHY symbol format, then the Pinetree software can be used to automatically switch between the two number representations. Referring to Figure 7, the same 8 integer values that were declared in the 'hsData' parameter of Figure 5 are now displayed in C-PHY symbol format. This was achieved by simply toggling the 'hsDataMode' from 'integer' to 'symbol'. Note that each integer now maps to 7 symbols as per the C-PHY mapping technology.

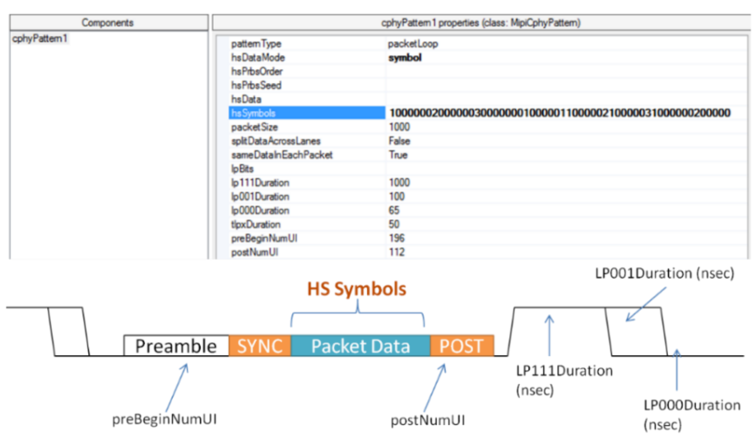


Figure 7: Toggling 'hsDataMode' to symbol automatically converts the packet payload data into C-PHY symbol representation.

MANIPULATING NON-PAYLOAD DATA PORTIONS OF A TRANSMISSION

In previous sections, we described how to manipulate payload data and global timing parameters of packet transmissions. What remains is to manipulate non-payload portions of a transmission. Namely, the SV3C-CPTX generator allows for sending invalid preamble data, sync word data, and post data. These are all additional parameters in the cphyPattern component as shown in Figure 8. Figure 9 and Figure 10 show how the timing parameters apply to these non-payload data transmissions.

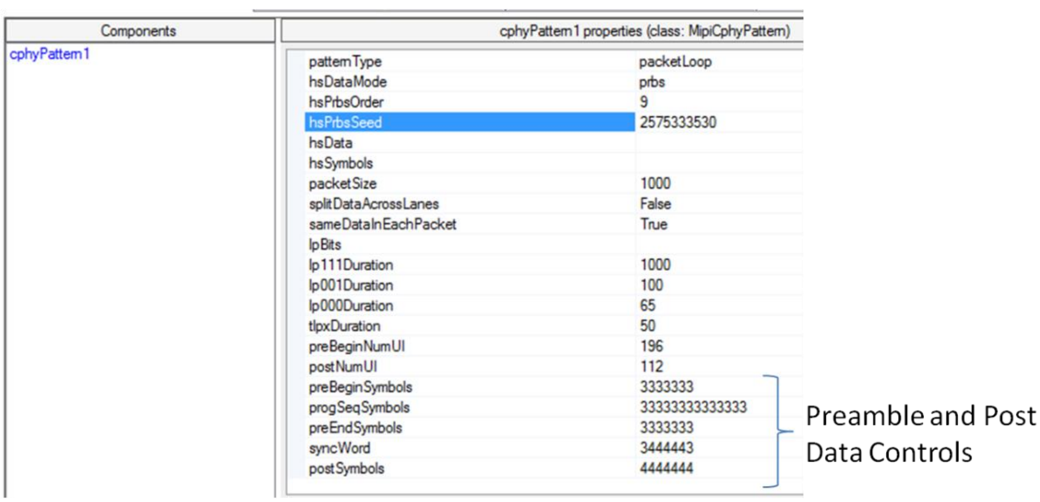


Figure 8: cphyPattern component showing how to manipulate non-payload portions of a transmission.

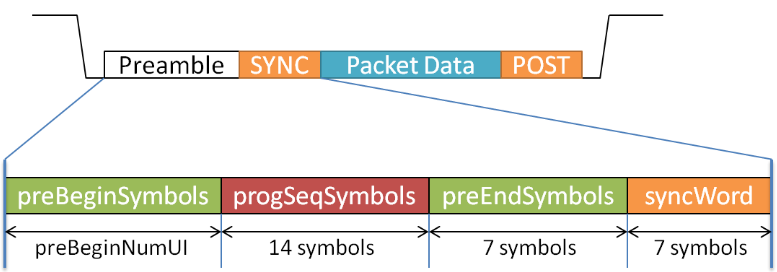


Figure 9: Description of non-payload data and timings.

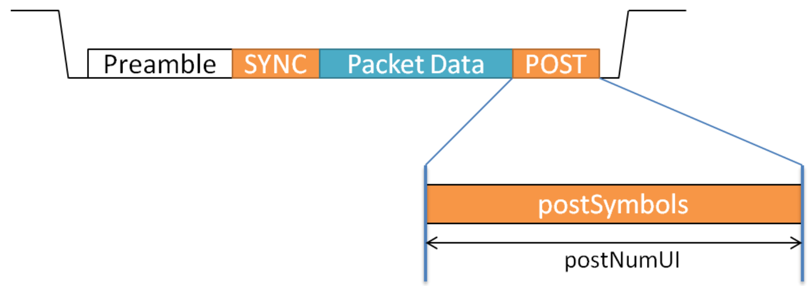
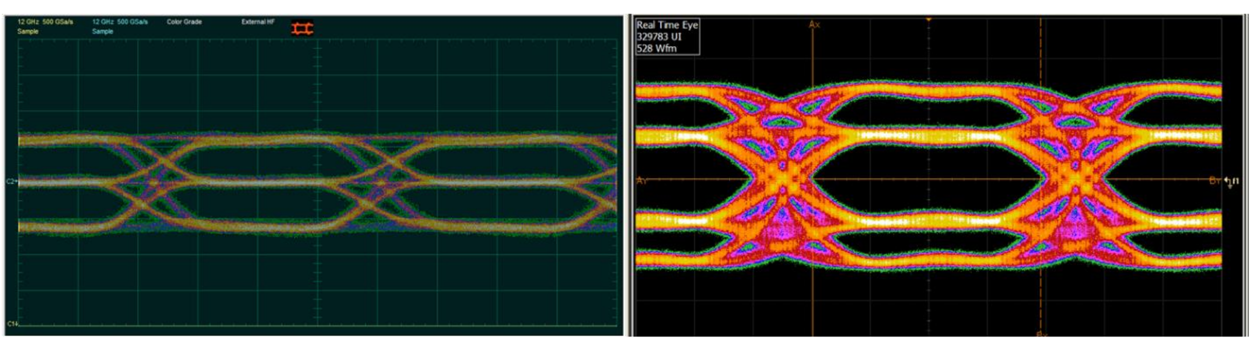


Figure 10: Description of non-payload data and timings.

ANALOG PARAMETER CONTROLS

As required by the C-PHY standard, each wire out of the SV3C-CPTX generator produces three-level single ended waveforms as shown in Figure 11(a). The span of the waveform (i.e. distance from the low level to the high level) is defined as single-ended voltage swing in this document, and it corresponds to the VOD specification in the C-PHY standard. Additionally, in order to enable receiver stressed eye testing, the generator includes common-mode control in which the entire waveform (low, mid, and high levels) is shifted up or down based on software commands (Figure 12). Similarly, all LP levels are programmable with fine resolution as shown in Figure 13. Such programmability is necessary for enabling various tests related to LP/HS interactions in C-PHY. Finally, advanced options exist for manipulating symmetry of the wire HS voltages (mid-level control), and these are all intended to help close the differential eye seen by a receiver (Figure 11(b)).



(a) (b)

Figure 11: (a) Single-ended waveform out of generator, and (b) differential signal seen by a C-PHY receiver connected to two wires out of the generator.

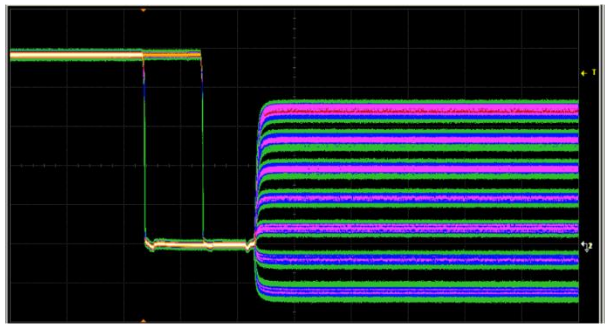


Figure 12: Illustration of HS common-mode signal control. Negative and positive voltages are produced.

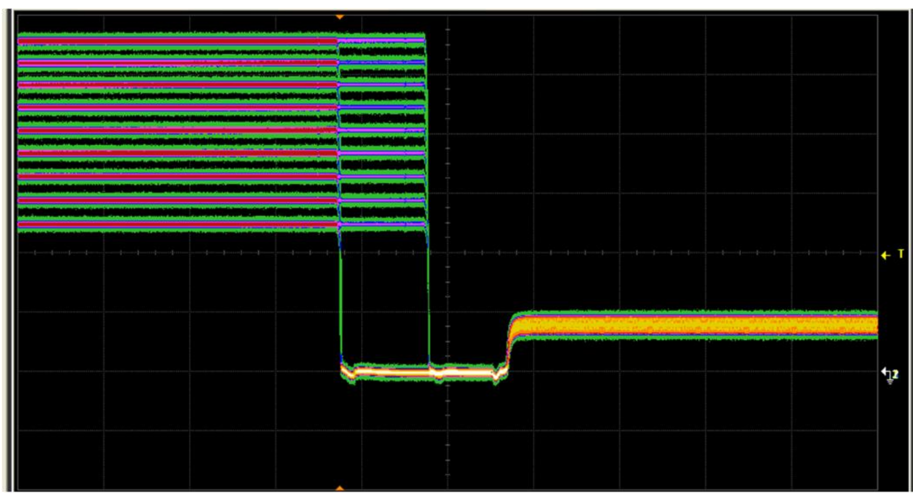


Figure 13: Illustration of LP signal level control. Negative and positive voltages are produced.

Coming back to receiver stressed eye testing, key to the SV3C-CPTX Generator functionality is the ability to perturb timings on the wires within a C-PHY lane individually. This allows for receiver stress signal calibration or for receiver stress testing. Figure 14 shows an example of the AB and BC differential eyes in which DCD is injected on one of the pairs. As can be seen, high precision eye closure (fraction of the symbol interval) is achieved and can be used to gradually stress a receiver until failure is observed. The SV3C-CPTX is able to create skew with a resolution of 1 ps or less and a range of about +/- 1 UI.

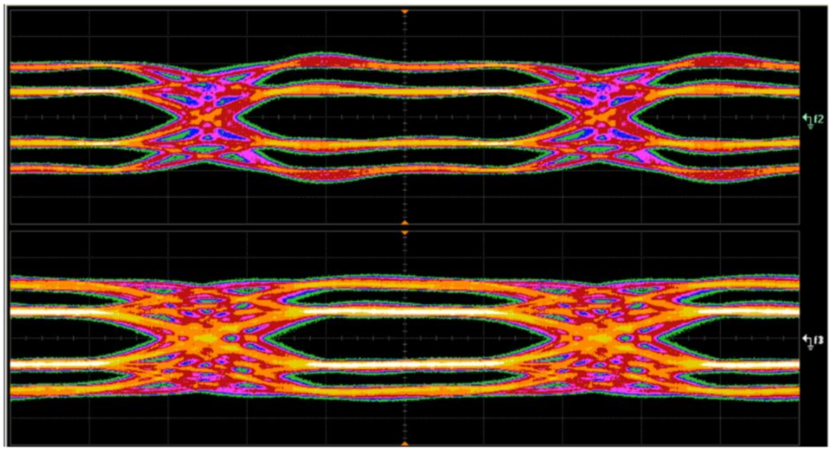
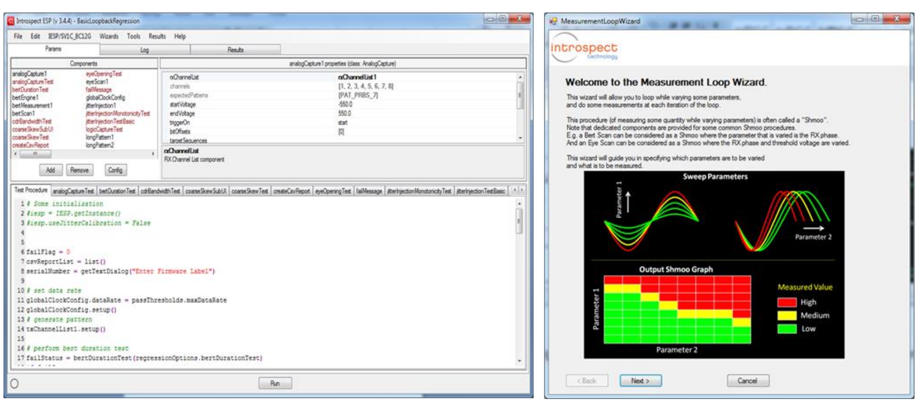


Figure 14: Differential AB and BC in which one of the eyes is closed with DCD injection.

AUTOMATION

The SV3C-CPTX C-PHY Generator is operated using the award winning Pinetree software. It features a comprehensive scripting language with an intuitive component-based design as shown in the screen shot in Figure 15(a). Component-based design is Pinetree's way of organizing the flexibility of the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, thus allowing program execution in a matter of minutes. For further help, the software environment features automatic code generation for common tasks such as Measurement Loop generation as shown in Figure 15(b).



(a) (b)

Figure 15: Screen captures of the Pinetree software user environment.

Physical Description and Pinout

Figure 16 shows a diagram of the physical ports of the SV3C-CPTX and Table 2 provides the physical dimensions for the unit. More detailed information on the SV3C-CPTX connectors and pinout is provided in Table 3.

Figure 16: Illustration of the SV3C-CPTX C-PHY Generator connectors.

TABLE 2: PHYSICAL DIMENSIONS

PARAMETER	VALUE
Length	9.5″ (241.3 mm)
Width	4.25″ (107.95 mm)
Height	1.3″ (33.3 mm)
Weight	2 lb

TABLE 3: LISTING OF SV3C-CPTX CONNECTORS

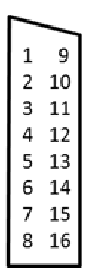
PORT / INDICATOR NAME	CONNECTOR TYPE
Ref Clock In Ref Clock Out A Ref Clock Out B	SMP Differential Pair SMP Differential Pair SMP Differential Pair
TX Lane 1 – 4	MXP (Lower Connector)
Replica Signals	MXP (Upper Connector)
12 pin Header Connector	–
USB Port	USB
Power Switch / Connector	–

The lower MXP connector, as shown in Figure, provides the TX Lane 1-4 output signals. The pin mapping for this lower connector is provided in Table 4 below.

The upper MXP connector provides four replica signals which may be connected directly to an external measurement device for live monitoring. The pin mapping for this upper connector is provided in Table 5 below.

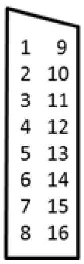
The 12 pin Header connector provides access to FPGA flag inputs and outputs as well as the Tear Effect Trigger for C-PHY signalling control. The pin mapping for this connector is provided in Table 6 below.

TABLE 4: MAPPING OF LOWER MXP CONNECTOR (LANE PINOUT)



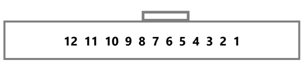
CONNECTOR PIN NUMBER	CORRESPONDING TX LANE
1,2,3	Lane 1 (A,B,C)
9,10,11	Lane 2 (A,B,C)
4,5,6	Lane 3 (A,B,C)
12,13,14	Lane 4 (A,B,C)

TABLE 5: MAPPING OF UPPER MXP CONNECTOR (REPLICA SIGNALS)



CONNECTOR PIN NUMBER	CORRESPONDING TX LANE
7	Lane 1 (A)
8	Lane 3 (A)
15	Lane 2 (A)
16	Lane 4 (A)

TABLE 6: MAPPING OF 12 PIN HEADER CONNECTOR



CONNECTOR PIN NUMBER	PIN DESCRIPTION
1	GPIO1 – FPGA Output
2	GPIO2 – FPGA Output
3	GPIO3 – FPGA Output
4	GPIO4 – FPGA Input
6	Tearing effect trigger - FPGA input

Specifications

TABLE 7: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol Support			
Physical layer interface	C-PHY		
MIPI protocol	CSI/DSI		Flexible pattern architecture allows for the generation of encoded PHY data or entire CSI/DSI frames
LP/HS Handling	Automatic		Tester automatically generates LP and HS data
Ports			
Number of Transmitter Lanes	4		
Number of Dedicated Clock Outputs	2		Separate clock for providing reference to the DUT
Number of Dedicated Clock Inputs	1		Used as external Reference Clock input
Number of Trigger Input Pins	3		Armed in software to trigger the start of specific measurements
Number of Flag Output Pins	3		Armed in software to flag test completion or pass/fail criteria
Data Rates and Frequencies			
Minimum Data Rate	80	Msps	
Maximum Data Rate	3.5	Gsps	
Minimum External Input Clock Frequency	10	MHz	
Maximum External Input Clock Frequency	250	MHz	
Minimum LP State Period	43	ns	LP period resolution is based on programmed HS data rate. Compiler

Maximum LP State Period	Software Programmable	ns	automatically selects period to satisfy user selection.

TABLE 8: TRANSMITTER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
HS Output Coupling			
Output Single-Ended Impedance	50	Ω	
Output Impedance Tolerance	+ / - 5	Ω	
HS Voltage Performance			
Minimum Single-Ended Output Voltage Swing	0	mV	
Maximum Single-Ended Output Voltage Swing	400	mV	
Voltage Resolution	10	mV	
Accuracy of Voltage Programming	larger of: +/- 5% of programmed value, and +/- 25mV	%, mV	
Rise and Fall Time Level Setting	90* Per-Wire	ps	* Optimized for C-PHY receiver testing
Per Wire HS Jitter Performance			
Random Jitter Noise Floor	1.5	ps	Based on measurement with a high-bandwidth real-time scope and with first-order clock recovery
Minimum Frequency of Injected Deterministic Jitter	0.1	kHz	

Maximum Frequency of Injected Deterministic Jitter	80	MHz	
Frequency Resolution of Injected Deterministic Jitter	0.1	kHz	
Maximum Peak-to-Peak Injected Deterministic Jitter	2	UI	
Magnitude Resolution of Injected Deterministic Jitter	500	fs	Jitter injection is based on multi-resolution synthesizer, so this number is an effective resolution. Internal synthesizer resolution is defined in equivalent number of bits
Accuracy of Injected Jitter Magnitude	larger of: +/-2% of programmed value, and +/-2 ps	%, ps	
HS Lane-to-Lane Skew Performance			
Lane to Lane Integer-UI Minimum Skew	-20	UI	
Lane to Lane Integer-UI Maximum Skew	20	UI	
Effect of Skew Adjustment on Jitter Injection	None		
HS Intra-Lane Wire-to-Wire Skew Performance*			* Limitations in range exist at low data rates
Minimum Wire to Wire Skew	-1	UI	
Maximum Wire to Wire Skew	1	UI	

Skew Injection Resolution	1	ps	
LP Voltage Controls			
Minimum Programmable Logic High Level	600	mV	
Maximum Programmable Logic High Level	2000	mV	* Extended range under investigation
Minimum Programmable Logic Low Level	-100	mV	
Maximum Programmable Logic Low Level	600	mV	
Logic Level Control Resolution	1	mV	
Logic Level Accuracy	Larger of 20mV or 5% of programmed value		

TABLE 9: CLOCKING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Internal Time Base			
Number of Internal Frequency References	1		
Frequency Resolution of Programmed Data Rate	1	Kbps	

TABLE 10: PATTERN HANDLING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Preset Patterns			
Standard Built-In Patterns	PRBS.5 PRBS.7 PRBS.9 PRBS.11 PRBS.13 PRBS.15 PRBS.18 PRBS.23 PRBS.31		
Pattern Choice per Transmit Channel	Per-transmitter		
User-programmable Pattern Memory			
Individual Force Pattern	Per-transmitter		
Minimum Pattern Segment Size	16	bits	
Maximum Pattern Segment Size	4G	Bytes	
Maximum Number of Unique Pattern Segments	128		
Total Memory Space for Transmitters	4G	Bytes	
Pattern Sequencing			
Sequence Control	Loop infinite		

	Loop on count		Count is a number that is specified later in this section
	Play to end		
Number of Sequencer Slots per Pattern Generator	16		Each pattern generator can string up to 16 different segments together, each with its own repeat count.
Number of Entry Slots	1		Separate from above 16 segments.
Number of Exit Slots	1		Separate from above 16 segments and entry slot.
Maximum Loop Count per Sequencer Slot	2^{16} - 1		
Additional Pattern Characteristics			
C-PHY Encoder & Mapper	Per Lane		
Escape Mode Command Entry	Per Lane		
Pattern Switching	Wait to end of segment Immediate		When sourcing PRBS patterns, this option does not exist.

TABLE 11: ENVIRONMENTAL CONDITIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Features			
Temperature Range	10 to 25	Celsius	Ambient temperature
Humidity Range	35 to 55	%	

REVISION NUMBER	HISTORY	DATE
1.0	Import from internal documentation	November 1, 2014
1.1	Formatting and typesetting	November 18, 2014
1.2	Updated figure 2, maximum data rate	November 20, 2014
1.3	Updated document template	June 10, 2015
1.4	Added 12-pin header connector information; updated Figure 16 and Table 2, updated Maximum data rate; added Table 1 ordering information	June 20, 2018
1.5	Updated document template	November 5, 2021
1.6	Updated software mentions for Pinetree	November 15, 2023
1.7	Updated Table 1, ordering part numbers; Updated Table 8 – HS Voltage Performance and LP Voltage Controls	February 22, 2024
1.8	Added Table 11 Environmental Conditions; Updated the Logic Level Accuracy in Table 8	September 19, 2024

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