introspect technology

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DATA SHEET

SV5C

Personalized SerDes Tester

C SERIES

Published in Canada on April 8, 2024
MK-D014E-E-24099

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Introduction

OVERVIEW

The SV5C is a parallel high-speed tester that meets the emerging test and validation requirements of increasingly complex electronic component and board designs. Operating at up to 12.5 Gbps and featuring 16 independent pattern generators and 16 independent signal/data analyzers, the SV5C is an all-in-one, phase-aligned bit error rate tester (BERT), providing self-contained functional and physical layer test and measurement capabilities for interfaces such as PCIe Gen 4, MIPI M-PHY, and USB3. The SV5C also includes unique technologies that allow it to tackle advanced protocols such as DDR4 and DDR5. The SV5C integrates multiple tools into one – providing unprecedented insight into crosstalk and channel-to-channel variations in highly parallel systems.

KEY BENEFITS

- High performance jitter tolerance testing in a handheld form factor
- Pattern generators offer per-lane voltage, timing, and noise injection controls
- Fully synthesized integrated jitter injection on all lanes
- Flexible pre-emphasis, equalization, and clock recovery per lane
- TX and RX phase alignment across all channels
- State of the art programming environment based on the highly intuitive Python language
- Single-ended or differential low-speed digital I/O for device under test control

APPLICATIONS

- ATE-on-Bench for DDR4 and DDR5 component, DIMM, and host-controller functional testing
- Parallel PHY validation of bus standards such as PCI Express (PCIe), MIPI M-PHY, XAUI, CPRI, JESD204B, USB, DDR4, and DDR5
- Mixed-technology applications such as high-speed ADC and DAC (JESD204) data capture and/or synthesis

PHYSICAL CONNECTIONS

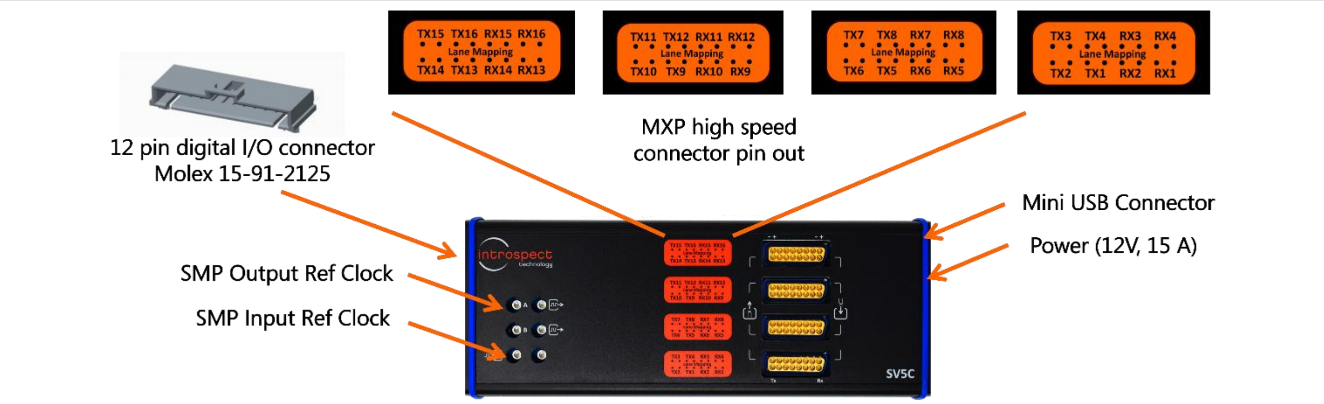
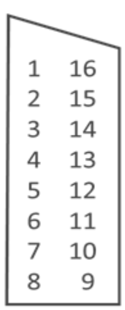


Figure 1: SV5C physical connections.

MXP HIGH SPEED CONNECTOR PINOUT

TABLE 1: SIGNAL MAPPING OF THE MXP CONNECTORS FOR SV5C

	MXP1 PIN	MXP1 SIGNAL	MXP2 PIN	MXP2 SIGNAL	MXP3 PIN	MXP3 SIGNAL	MXP4 PIN	MXP 4 SIGNAL
MXP Top View 	1	RX4P	1	RX8P	1	RX12P	1	RX16P
	2	RX4N	2	RX8N	2	RX12N	2	RX16N
	3	RX3P	3	RX7P	3	RX11P	3	RX15P
	4	RX3N	4	RX7N	4	RX11N	4	RX15N
	5	TX4P	5	TX8P	5	TX12P	5	TX16P
	6	TX4N	6	TX8N	6	TX12N	6	TX16N
	7	TX3P	7	TX7P	7	TX11P	7	TX15P
	8	TX3N	8	TX7N	8	TX11N	8	TX15N
	9	TX2N	9	TX6N	9	TX10N	9	TX14N
	10	TX2P	10	TX6P	10	TX10P	10	TX14P
	11	TX1N	11	TX5N	11	TX9N	11	TX13N
	12	TX1P	12	TX5P	12	TX9P	12	TX13P
	13	RX2N	13	RX6N	13	RX10N	13	RX14N
	14	RX2P	14	RX6P	14	RX10P	14	RX14P
	15	RX1N	15	RX5N	15	RX9N	15	RX13N
	16	RX1P	16	RX5P	16	RX9P	16	RX13P

ORDERING INFORMATION

TABLE 2: ITEM NUMBERS FOR THE SV5C AND RELATED PRODUCTS

PART NUMBER	NAME	KEY DIFFERENTIATORS
5712	SV5C-12 SerDes Tester	Per channel skew and jitter injection control, 12.5 Gbps maximum data rate
5713	SV5C-12 SerDes Tester (2 x 16 Channel Instruments)	Two-pack order code for receiving a complete 32-channel memory interface test solution. Consists of two 5712 instruments and associated calibration data
5779	DDR5 Reference Termination Board	Termination board for measuring DDR5 signals on either an oscilloscope or an SV5C
5780	Bidirectional Communications Kit	Kit for enabling bidirectional DQ/DQS bus communications on SV5C
7206	SV6E-X Mid-Frequency Digital Test Module – I3C	Multi-protocol digital exerciser and analyzer with 200 MHz I/O speeds

Features

TRANSMIT BUFFER

The transmit buffer in the SV5C is designed to enable full receiver test coverage while also allowing for maximum flexibility to interface to various device types. A simplified block diagram of the transmit buffer is shown in **Figure 2**. Each channel in the SV5C includes a programmable DC common-mode termination level, a programmable signal swing, and a programmable slew rate. Similarly, delay and noise generators enable fine static skew control, dynamic jitter control, and difference mode or common-mode AC noise control. Finally, each transmit buffer includes a 4-tap FIR filter for emulating device de-emphasis waveforms or for adjusting output signal waveform shape.

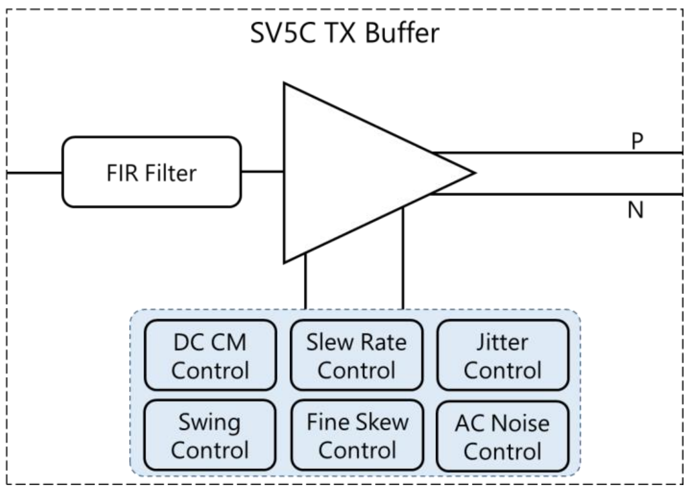


Figure 2: Transmit buffer controls in the SV5C.

Each transmit buffer in the SV5C is programmed independently of other channels and independently of any pattern payload or functional protocol operation. This allows for automated receiver test sweeps under the most realistic conditions. For example, a receiver minimum sensitivity test can be performed on a DDR5 DQ or DQS signal while all neighboring signals are toggling at maximum voltage swing.

NOTE

The SV5C transmit buffer can operate in single-ended mode. Please refer to application-specific documentation for further information.

RECEIVE BUFFER

Just like the transmit buffer, the SV5C receive buffer is designed to enable sophisticated signal measurement features while functionally interoperating with various device types and signaling interfaces. As shown in **Figure 3**, each receive buffer has a programmable continuous-time linear equalizer (CTLE) block, and this helps recover closed eyes at high data rates. More importantly, the receive buffer offers dynamic termination control, and it is able to operate in high-impedance mode while performing functional data captures. Finally, the SV5C receive buffer contains a window comparator with programmable threshold voltage and sampling phase controls.

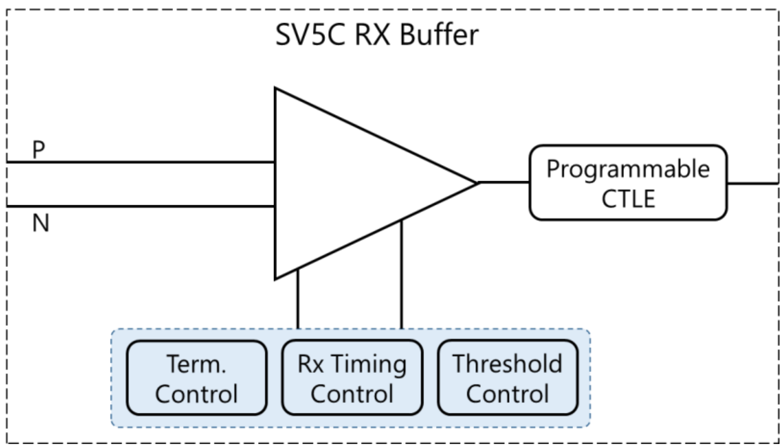


Figure 3: Receive buffer controls in the SV5C.

Each receive buffer can be programmed independently of other channels and independently of any pattern payload that is being received. At the same time, the protocol capable machines inside the SV5C hardware and software are all able to automatically control the receive buffers, thus tremendously facilitating functional testing. That is, all receive buffer parameters are typically set automatically by the various pre-built functions in the SV5C and in Pinetree.

NOTE

For DDR5 or LPDDR5 DQ and DQS functional testing, the SV5C receive buffer works with the Bidirectional Kit, which transforms the SV5C into a full-duplex data bus. The Bidirectional Kit also provides programmable reference termination levels to a component or DIMM under test.

SYSTEM CLOCKING

Figure 4 illustrates the global clocking network in the SV5C. A single reference clock source is used to drive the entire system, and this source can be internal or external (driven through the Clk In port). The master clock source is routed to three high-accuracy and low-jitter fractional-N synthesizers:

- Synth1 drives the main tester channels and provides the time base for all 16 transmit and receive channels
- Synth2 provides the ability to generate arbitrary external reference clocks that are synchronized to the Clk In port
- Synth3 provides the same capability as Synth2, thus resulting in two output reference clocks per SV5C

Each of the 16 tester channels contains precision timing synthesis blocks that are used for generating frequency drifts, static skews, dynamic skews (and jitter), and bit slips.

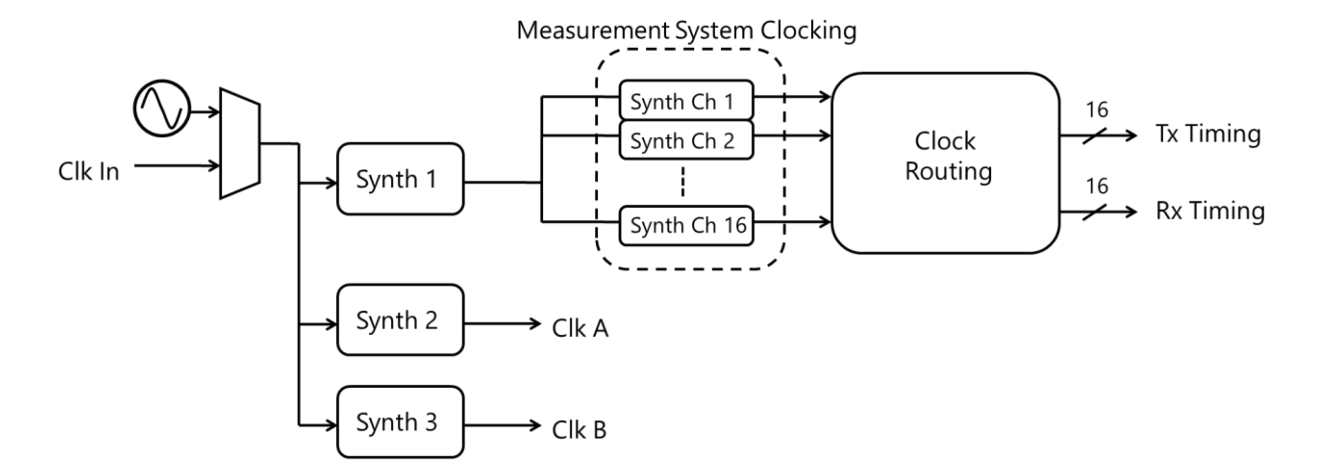


Figure 4: Global clock network in the SV5C.

NOTE

When cascading two or more SV5C systems to create a wide test bus, the Clk In, Clk A, and Clk B are used to ensure 0-ppm synchronization between all the SV5C testers. Specifically, the master SV5C is used to generate reference clocks that are routed to the Clk In ports of the slave SV5C units.

PATTERN HANDLING

The SV5C contains several pattern provider tools for generating and/or receiving test patterns. At the basic fixed-pattern level, the SV5C can generate any PRBS polynomial as well as any user-defined pattern. In addition, the SV5C contains nested pattern sequencers in which 16 separate pattern blocks can be programmed with arbitrary repetition counts and then these repeated blocks can be inserted into an outer repetition loop.

Perhaps most importantly, the SV5C contains protocol aware features that allow for the creation of functional command sequences. These features are encapsulated in Pattern Timeline tools, an example of which is shown in **Figure 5**. This tool contains repeats, pauses, branched commands, and triggers based on received protocol traffic or received programming commands. The net result is that the SV5C can perform complete functional testing, thus resulting in a highly effective ATE-on-Bench solution for wide-bus applications.

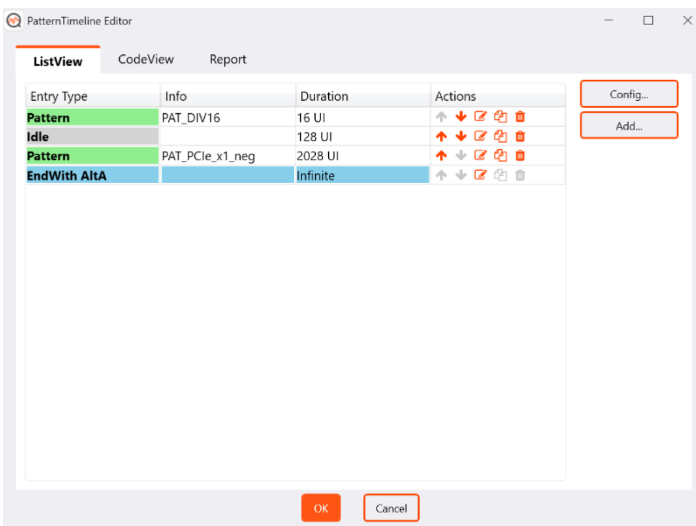


Figure 5: Pattern timeline editor illustrating the ability to create complex timing and command sequences.

NOTE

For DDR4, DDR5, or LPDDR5 applications, the SV5C contains dedicated command compliers based on the Pattern Timeline tool. These compilers support component buses such as the RCD command and address bus or host controller buses such as the DQ/DQS bus. Further information is available in the context help menus within the Pinetree GUI.

STANDARD ERROR DETECTOR ANALYSIS

The SV5C instrument has an independent Bit Error Rate Tester (BERT) for each of its input channels. Each BERT compares recovered (retimed) data from a single input channel against a specified data pattern and reports the bit error count.

Apart from error counting, the instrument offers a wide range of measurement and analysis features including:

- Jitter separation
- Eye mask testing
- Voltage level, pre-emphasis level, and signal parameter measurement
- Shmoos of various kinds

Figure 6 illustrates a few of the analysis and reporting features of the SV5C. Starting from the top left and moving in a clockwise manner, the figure illustrates bathtub acquisition and analysis, waveform capture, eye diagram plotting and raw data viewing. As always, these analysis options are executed in parallel on all activated lanes.

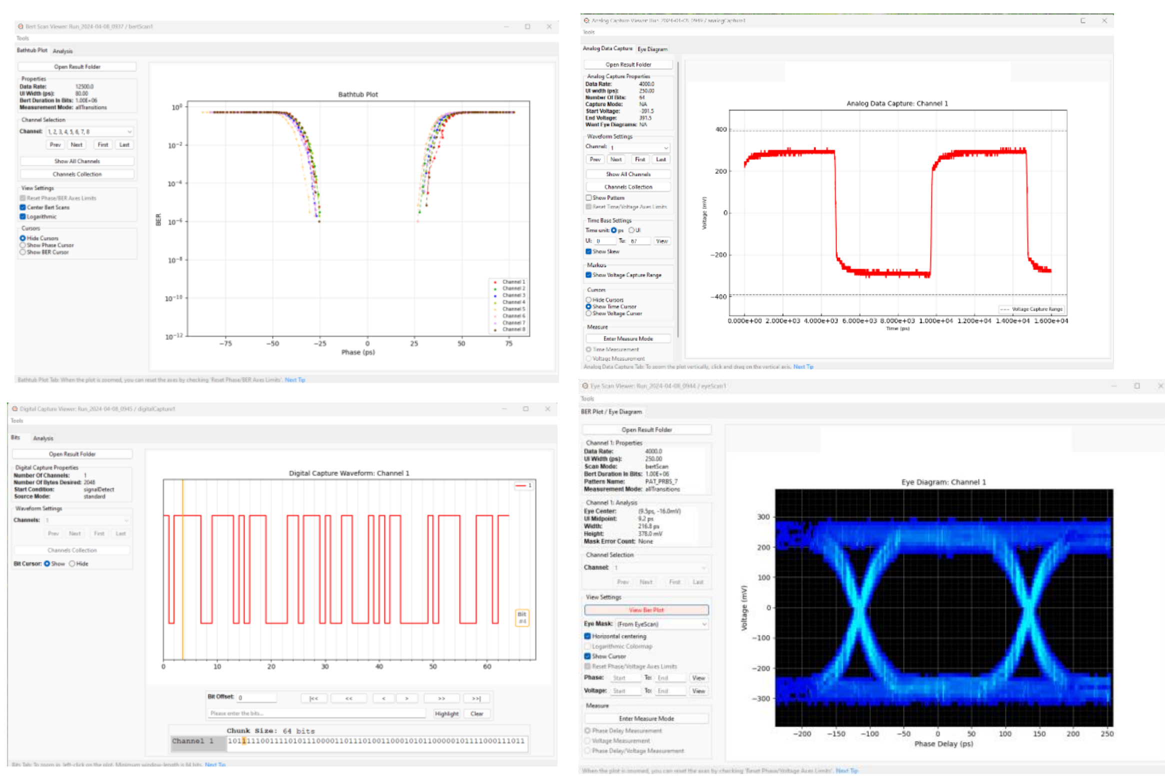


Figure 6: Collection of standard error detector tools in the SV5C.

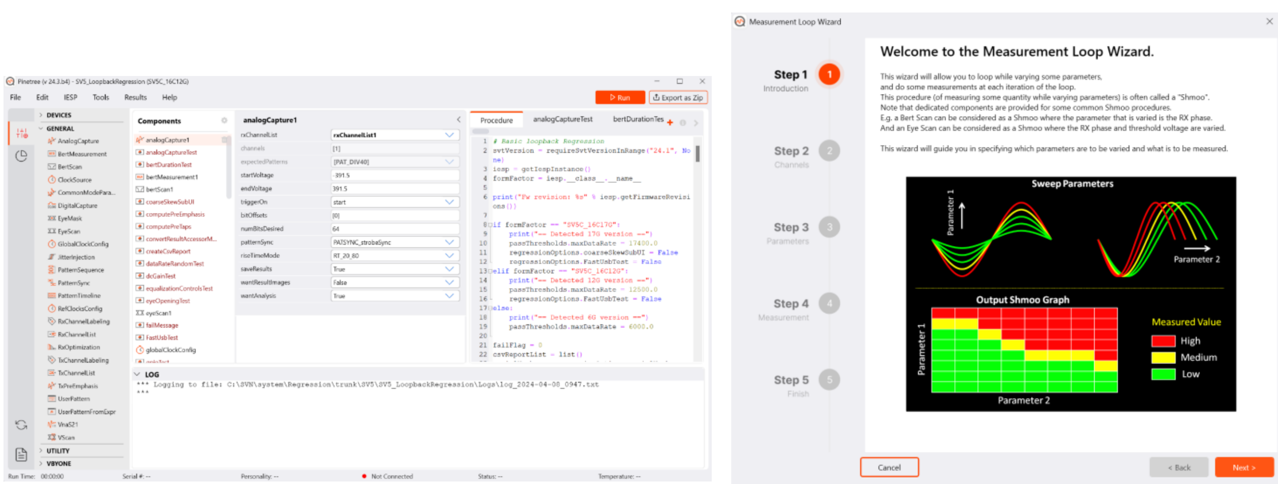
AUXILIARY DEVICE CONTROLS

The SV5C contains general purpose I/O pins for controlling devices under test or driving sideband bus signals. Of these pins, the following classes of functions are available:

- Trigger and flag pins for starting patterns, capturing patterns, or reporting test results
- I2C/I3C master pins (SDA/SCL) for controlling devices such as DDR5 power management integrated circuits (PMIC) or sensors
- Daisy-chain trigger in and trigger out pins for cascading and aligning multiple SV5C units together. These daisy chain signals work in conjunction with the Clk In, Clk A, and Clk B signals to align any number of SV5C units together

AUTOMATION

The SV5C is operated using Introspect's award-winning software, Pinetree. It features a comprehensive scripting language with an intuitive component-based design as shown in the screen shot in **Figure 7**(a). Component-based design is Pinetree's way of organizing the flexibility of the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, thus allowing program execution in a matter of minutes. For further help, the SV5C features wizard-based code generation for highly automated tasks such as measurement loops (illustrated in **Figure 7**(b)).



(a) (b)

Figure 7: Screen captures of Pinetree.

Specifications

TABLE 3: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Ports			
Number of Transmitters	16		Capable of single-ended operation
Number of Receivers	16		Capable of single-ended operation
Number of Dedicated Clock Outputs	1		Individually synthesized frequency and output format
Number of Dedicated Clock Inputs	1		Used as external reference clock input
Number of Trigger Inputs	2		
Number of Flag Outputs	2		
Number of I2C/I3C Masters	1		
Power			
DC Input Voltage	12	Volt	
Current Draw	5.7	Amp	5 Gbps / 16 channel TX and RX operation
	6.6	Amp	12.5 Gbps / 16 channel TX and RX operation
Data Rates and Frequencies			
Minimum Programmable Data Rate	0.763	Mbps	
Maximum Programmable Data Rate	12.5	Gbps	
Maximum Data Rate Purchase Options	12.5	Gbps	
Data Rate Field Upgrade	Yes		License to change speed grade is available for purchase at any time
Frequency Resolution of Programmed Data Rate	1	kHz	Finer resolution is possible. Contact factory for customization
Minimum External Input Clock Frequency	25	MHz	

Maximum External Input Clock Frequency	250	MHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)
Minimum Output Clock Frequency	10	MHz	
Maximum Output Clock Frequency	500	MHz	
Output Clock Frequency Resolution	1	kHz	
Supported External Input Clock I/O Standards			Support for LVDS, LVPECL, CML, HCSL, and LVCMOS

TABLE 4: TRANSMIT BUFFER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Output Coupling			
Output Differential Impedance	100	Ohm	
Differential Impedance Tolerance	+/- 10	Ohm	
Output Single-Ended Impedance	50	Ohm	
Single-Ended Impedance Tolerance	+/- 5	Ohm	
Output Voltage Performance			
Minimum Single-Ended Voltage Swing	0	V	Can achieve true idle signaling
Maximum Single-Ended Voltage Swing	490	mV	
Voltage Swing Resolution	10	mV	
Voltage Swing Accuracy	>10% or 10 mV	%, mV	
Minimum Common Mode Voltage	-20	mV	
Maximum Common Mode Voltage	750	mV	
Common Mode Voltage Resolution	1	mV	

Common Mode Voltage Accuracy	>20% or 20 mV	%, mV	
Swing and Common Mode Setting	Per Lane		
Rise Time	30	ps	
Fall Time	30	ps	
Slew Rate Range	13	V/ns	This is defined as the difference between the fastest slew rate and the slowest slew rate
De-Emphasis Performance			
Pre-Tap 1 Range	+/- 150	mV	FIR taps defined as additive increments
Pre-Tap 1 Resolution	10	mV	
Post-Tap 1 Range	+/- 300	mV	
Post-Tap 1 Resolution	10	mV	
Post-Tap 2 Range	+/- 150	mV	
Post-Tap 2 Resolution	10	mV	
De-Emphasis Setting	Per Lane		
Jitter and Noise Performance			
RJ (RMS)	700	fs	Based on a sampling oscilloscope measurement with first order clock recovery
Minimum Frequency of SJ	0.1	kHz	
Maximum Frequency of SJ	50	MHz	
Frequency Resolution of SJ	0.1	kHz	
Maximum Peak to Peak SJ	16000	ps	Numerically generated. Only tested to 1000 ps
Magnitude Resolution of SJ Programming	500	fs	
Accuracy of Injected SJ	>10% or 10 ps	%, ps	
Number of SJ Sources per Channel	2		
Maximum Amplitude of Common Mode Noise	40	mV	

Maximum Amplitude of Difference Mode Noise	80	mV	
Amplitude Resolution of Injected Noise	1	mV	
Maximum Frequency of Injected Noise	1	GHz	
Channel Skew Performance			
Minimum Coarse Skew	-20	UI	
Maximum Coarse Skew	+20	UI	
Coarse Skew Resolution	0.5	UI	Data rates < 6.25 Gbps
Coarse Skew Resolution	1	UI	Data rates >= 6.25 Gbps
Minimum Fine Skew	-500	ps	Testing limit – hardware is capable of larger skews
Maximum Fine Skew	+500	ps	Testing limit – hardware is capable of larger skews
Fine Skew Resolution	1	ps	
Channel to Channel Auto Alignment Accuracy	20	ps	Across 16 channels

TABLE 5: RECEIVE BUFFER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Input Coupling			
Input Differential Impedance	100	Ohm	
Differential Impedance Tolerance	+/- 10	Ohm	
Input Single-Ended Impedance	50	Ohm	
Single-Ended Impedance Tolerance	+/- 5	Ohm	
High-Impedance Programming	Per Lane		Dynamically programmable within Pattern Timeline
Comparator Performance			
Minimum Threshold Voltage	-400	mV	
Maximum Threshold Voltage	+400	mV	

Threshold Voltage Resolution	20	mV	
Threshold Voltage Accuracy	>15% or 15 mV	%, mV	
Minimum Detectable Differential Voltage	90	mV	
Maximum Allowable Differential Voltage	1200	mV	
Resolution Enhancement			
DC Gain Settings	0, 3, 6, 8, 10	dB	
CTLE High Frequency Settings	0 … 15	dB	
DC Gain Settings	Per Lane		
CTLE Settings	Per Lane		
Receiver Jitter Performance			
RMS Jitter Noise Floor (<6.25 Gbps)	2	ps	RMS
RMS Jitter Noise Floor (>6.25 Gbps)	1	ps	RMS
Timing Generator Performance			
Timing Resolution	7.8125	mUI	Measured at 12.5 Gbps
	3.90625	mUI	Measured at 6.25 Gbps
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	Unlimited		

TABLE 6: CLOCKING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Internal Time Base			
Number of Internal Frequency References	1		
Frequency Resolution of Programmed Data Rate	1	kbps	
Clock Recovery			
Tracking Bandwidth	20	MHz	
Clock Recovery Setting	Per Lane		Can be disabled for source synchronous applications
SSC Tracking Bandwidth	33	kHz	
SSC Tracking Spread	0.5	%	

TABLE 7: PATTERN HANDLING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
PRBS Patterns			
Polynomials	5,7,9,11,13,15,21,31		
PRBS Generator Setting	Per Lane		
Pattern Sequencer			
Entry and Exit Slots	Yes		
Number of Inner Slots	16		
Repeat Count Per Slot	65536		
Repeat Count for Outer Loop	65536		Outer loop can encompass any number of slots, up to all 16 slots
Pattern Timeline			
Hold States	Alt A		
	Alt B		

	All Ones		
	All Zeros		
	Idle		
	Wait for Trigger		
	Wait for Received Word		
	Wait for Software Command		
Hold State Setting	Per Lane		

REVISION NUMBER	HISTORY	DATE
1.0	Document release	September 4, 2018
1.1	Updates to overview and specifications	September 11, 2018
1.2	Updated document template	March 3, 2020
1.3	Updated data rates and updated software mentions with Pinetree	September 7, 2023
1.4	Updated Table 1 for RX9P; Table 3 (data rates, number of dedicated clock outputs); Figure 1; Table 2 for adding part number for SV6E-X	April 5, 2024
1.5	Updated the software screenshots	April 8, 2024

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