



### **PRODUCT BRIEF**

# M SERIES M5512 GDDR7 Memory Test System



### ATE on Bench for GDDR7 Characterization and Test

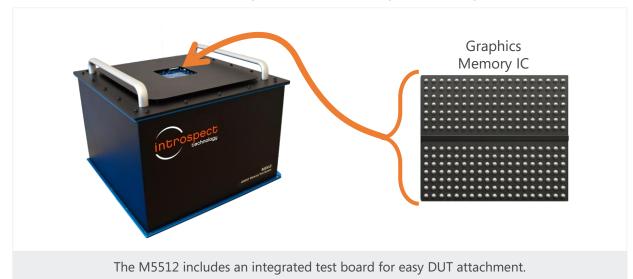
The M5512 GDDR7 Memory Test System is a category-creating solution for characterizing and functionally testing memory integrated circuits based on the JEDEC Graphics Double Data Rate 7 SGRAM Standard (GDDR7). Featuring high-speed, bidirectional PAM3 signaling, low-speed NRZ signaling, and complete protocol training capability, this solution is the optimal tool to help bring next-generation graphics memory to the industry.

#### **KEY FEATURES:**

- **Complete memory testing:** connects to all channels in a single graphics memory IC, thus providing test coverage on all pins
- Programmable device power supplies: precision programming of the power up and power down sequence of the memory IC under test
- Superior signal integrity: world-class pinelectronics running at 40 Gbps in PAM3 mode
- AC characterization: picosecond resolution timing and mV resolution shmoo capability

#### **KEY BENEFITS:**

- Fastest time to market: perform deep memory read/write operations and characterize electrical and timing specifications
- Most capable PAM3 signaling: leveraging years of expertise in SerDes technology, the PAM3 pinelectronics exceed the requirements of the GDDR7 specifications
- Automated: scripting capability ideal for debug tasks, verification, and full-fledged production screening of devices and system boards



### Access to Every Pin and Every Memory Cell



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M5512 GDDR7 Test System

## Native GDDR7 Virtual Memory Controller

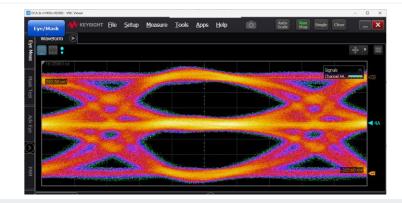
	Components 🔅	gddrController1		<	Procedure
	<ul> <li>gddrBdkChannelLabeling1</li> <li>gddrChannelLabeling1</li> <li>gddrChannelLabeling2</li> </ul>	deviceSerialNum	rdimm0		<pre>1 globalClockConfig.setup() 2 gddrController1.run()</pre>
		phyParams	gddrPhyParams1	$\checkmark$	
		gddrParams	gddrParams1	$\checkmark$	
	🛹 gddrController1 👘	rxChannelLabeling	gddrChannelLabeling1	$\checkmark$	
	¦†¦ gddrParams1	txChannelLabeling	gddrChannelLabeling2	$\checkmark$	
	+++ gddrPhyParams1	bdkChannelLabelings	gddrBdkChannelLabeling1		
	OglobalClockConfig	calibrateZq	True	$\checkmark$	
		trainingDataCaPhase	auto	$\sim$	

Focus on your test algorithms and let the M5512 virtual memory controller manage the protocol.

# Specifications

PARAMETER	VALUE	UNITS	DESCRIPTION	
Maximum NRZ Data Rate	20	Gbps	Exceeds JEDEC specifications	
Maximum PAM3 Data Rate	40	Gbps	Exceeds JEDEC specifications	
Tx Phase Setting Resolution	1	ps	Per-pin phase control	
Rx Phase Setting Resolution	1.5	ps	Per-pin phase control	
Voltage Range	0-1.2	V	Per-pin voltage control	
Tx Voltage Setting Resolution	10	mV	Enables sensitivity testing	
Rx Voltage Resolution	10	mV	Enables eye diagram testing	

# Physical Layer Performance: 40 Gbps PAM3 Eye Diagram



Achieve high-confidence memory testing with the M5512's superior signal integrity.